

Substrats bio-sourcés pour une électronique à faible impact environnemental

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Outline



- A. Substrats pour une électronique soutenable
- B. Substrat PLA-Lin pour une application numérique haute fréquence
- C. Module de puissance chip-on-chip

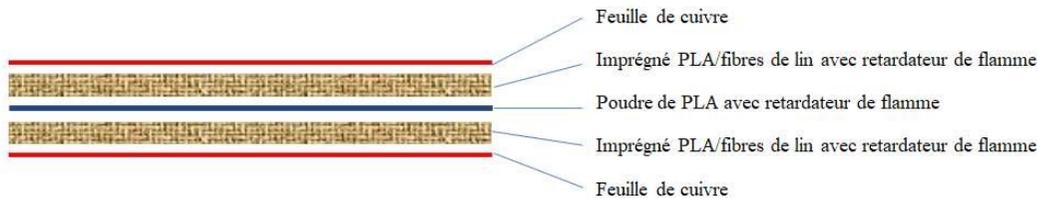
Substrats pour une électronique soutenable

- **Bio-sourcé, Bio-dégradable / recyclable ?**

- Lien avec la récupération des métaux -> bio-lixivation, récup. composants
- Quel cycle de vie ?

- **Quelques exemples :**

- Bio-epoxy (huiles lin/soja) + fibres lin [1]
- Gluten + fibres Bananes [2]
- **PLA + fibres de lin [3]**



Substrat PCB PLA-Lin (Meshlin Composites)

N° lot	Fréquence (MHz)	ϵ_r	$\tan(\delta)$
1	930	2,49±0,17	0,05±0,01
1	2480	2,31±0,16	0,04±0,01
2	1200-9470	2,18±0,16	NC

FR4 ref: /2 (pointing to ϵ_r) FR4 ref: x2 (pointing to $\tan(\delta)$)

Caractérisation en cavité RF

[1] John D. Lincoln, Andrew A. Shapiro, James C. Earthman, Jean-Daniel M. Saphores, and Oladele, (2008), — Design and Evaluation of Bioepoxy-Flax, Composites for Printed Circuit Boards, IEEE Transactions On Electronics Packaging Manufacturing, 31(3), 211.

[2] Guna, V. K., Murugesan, G., Basavarajaiah, B. H., Ilangovan, M., Olivera, S., Krishna, V., & Reddy, N. (2016). Plant-based completely biodegradable printed circuit boards. *IEEE Transactions on Electron Devices*, 63(12), 4893-4898.

[3] A. Géczy et al., "Novel PLA/Flax Based Biodegradable Printed Circuit Boards," 2022 45th International Spring Seminar on Electronics Technology (ISSE), Vienna, Austria, 2022, pp. 1-6, doi: 10.1109/ISSE54558.2022.9812827.

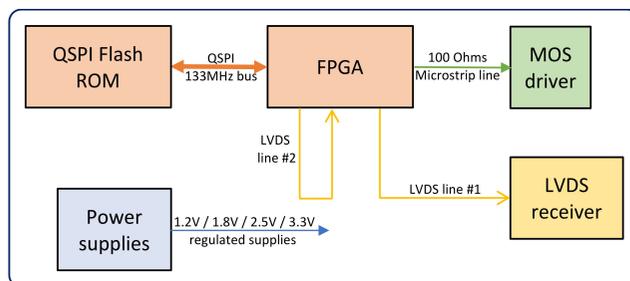
Circuit numérique rapide sur substrat PLA-Lin

• Adapter le design

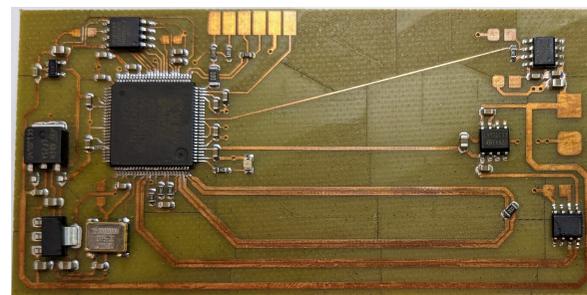
- Impédance des lignes adaptées (LVDS sur paire différentielle, ligne micro-strip)
- Limitations pour les technos traversantes
- Limitations pour le choix des boitiers
- Autres limitations liées à la rigidité du substrat

• Adapter la fabrication

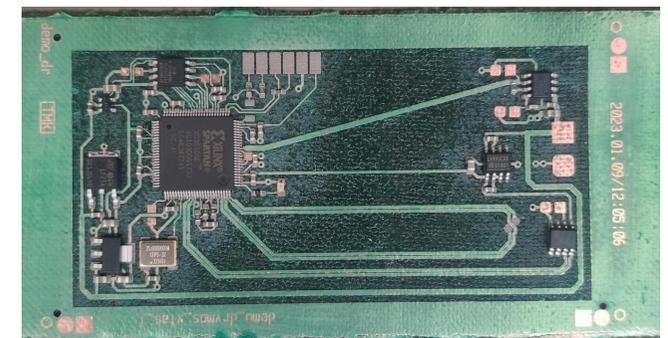
- Testé avec gravure laser
- $T_g = 57^\circ \text{C} \Rightarrow$ brasure alliage SnBi (138°), Brasage phase vapeur (VPS)
- Reprise manuelle possible (220°)
- Métalisation des vias ?
- Protéger contre la bio-dégradation
- Multicouches ?



GT PCB – 2 février 2023



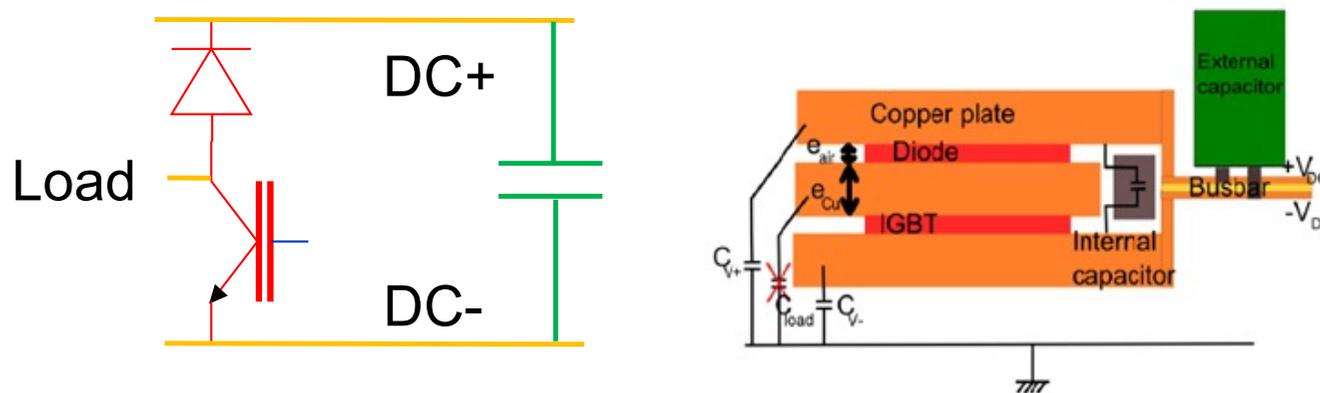
Design de référence sur FR4



Design adapté, sur PLA/lin

Power Chip-On-Chip (PCOC)

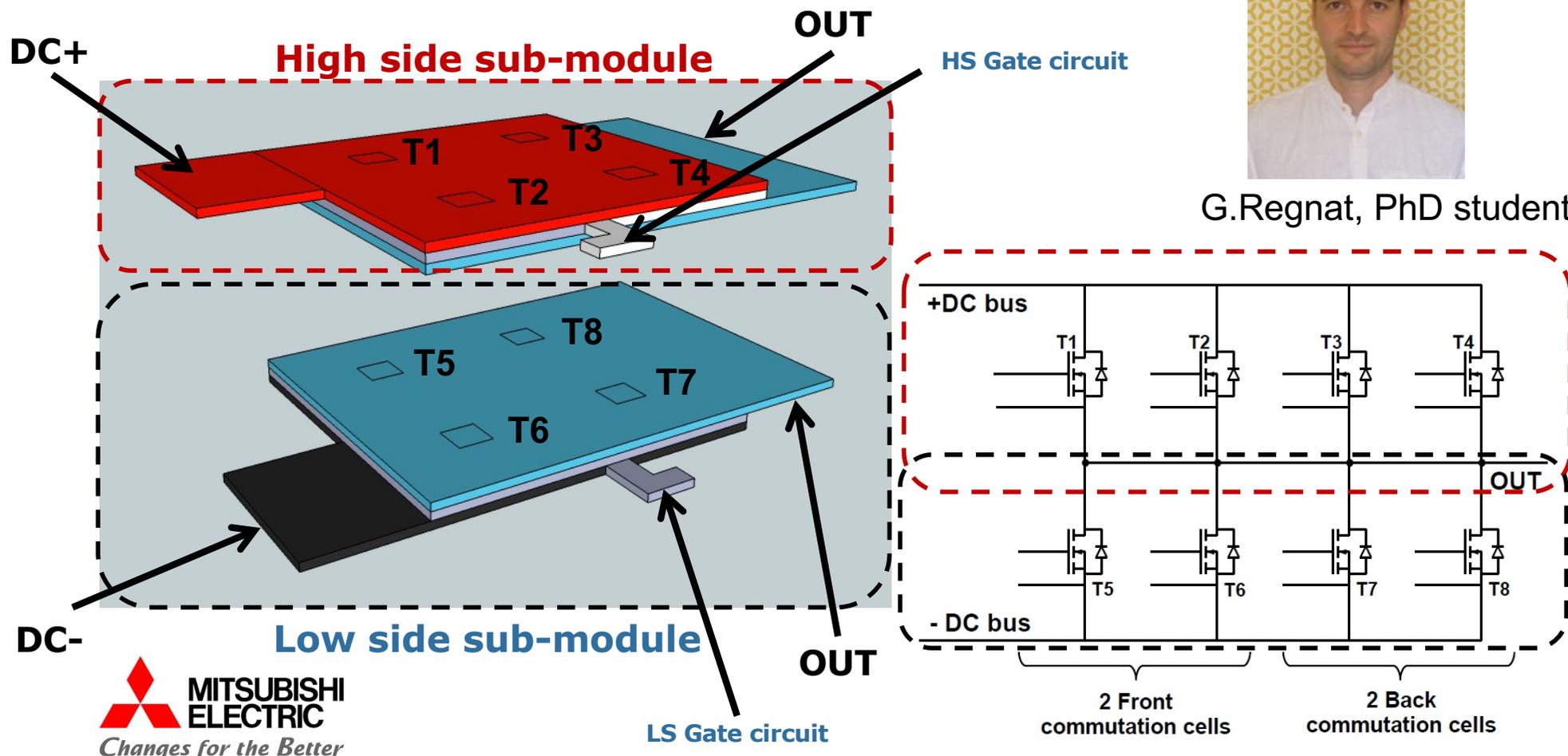
- **3D integration of the converter for vertical components**
- **Main goal: reduction of the stray inductance and of the common mode stray capacitance**



The stray inductance is minimized due to the global integration as part of the busbar itself

PCOC Module with PCB Embedded Die Process

Prototype overview

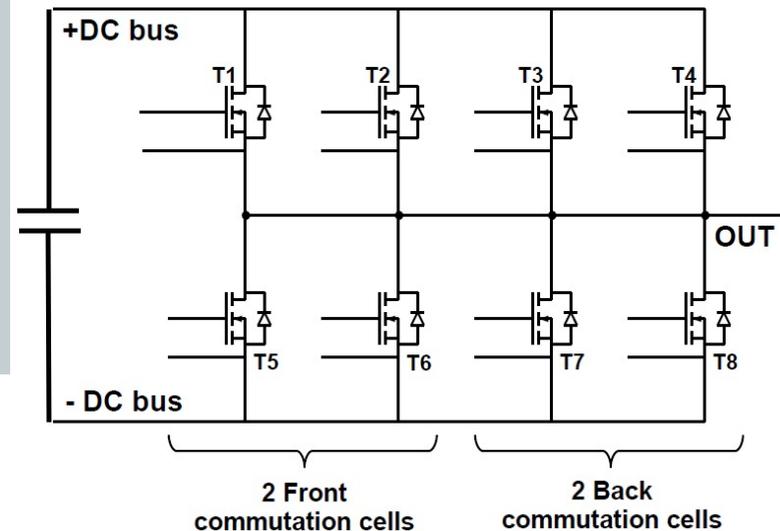
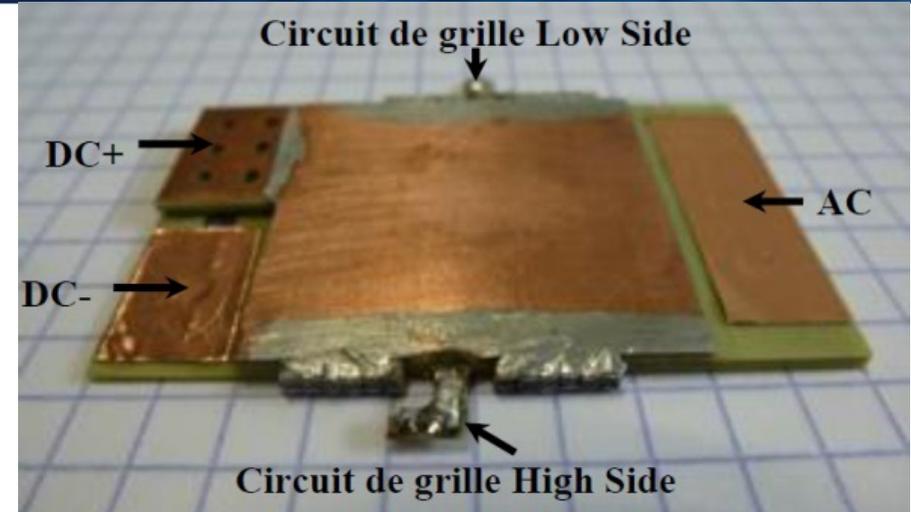
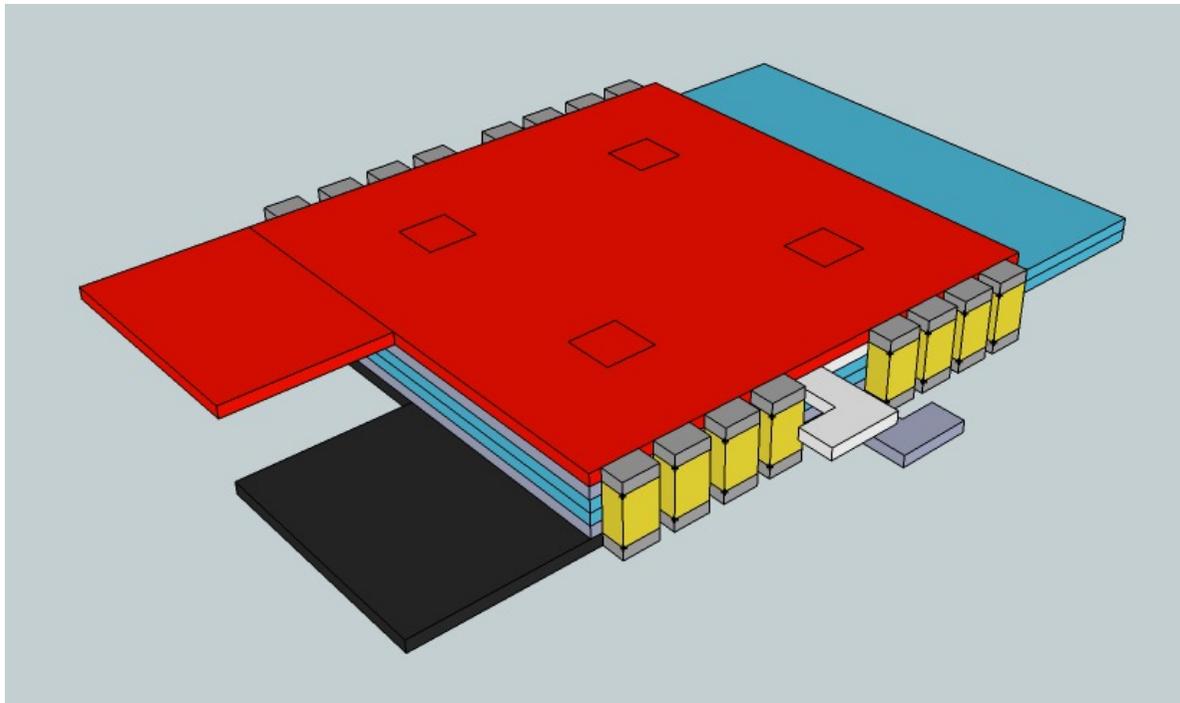


G. Regnat, PhD student



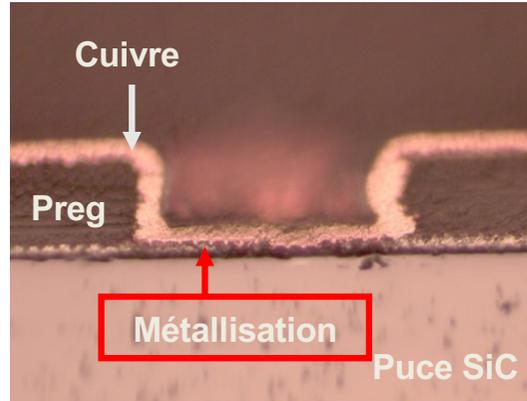
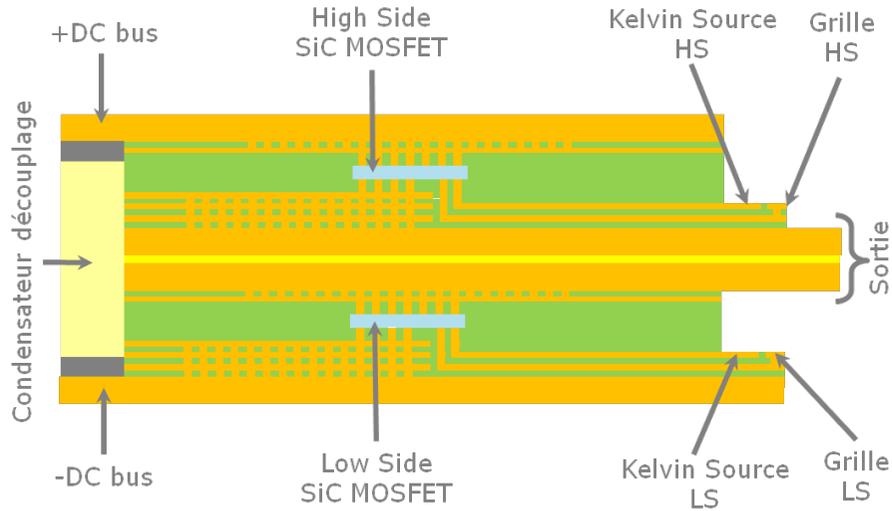
PCOC Module with PCB Embedded Die Process

Prototype overview



PCOC Module with PCB Embedded Die Process

Power and Gate circuits

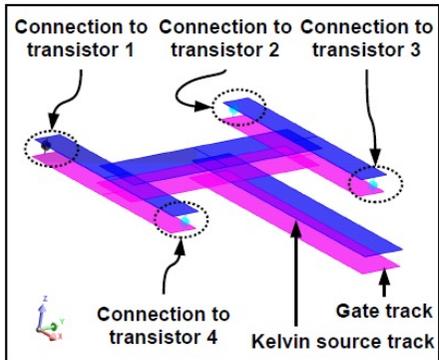


Source connection:

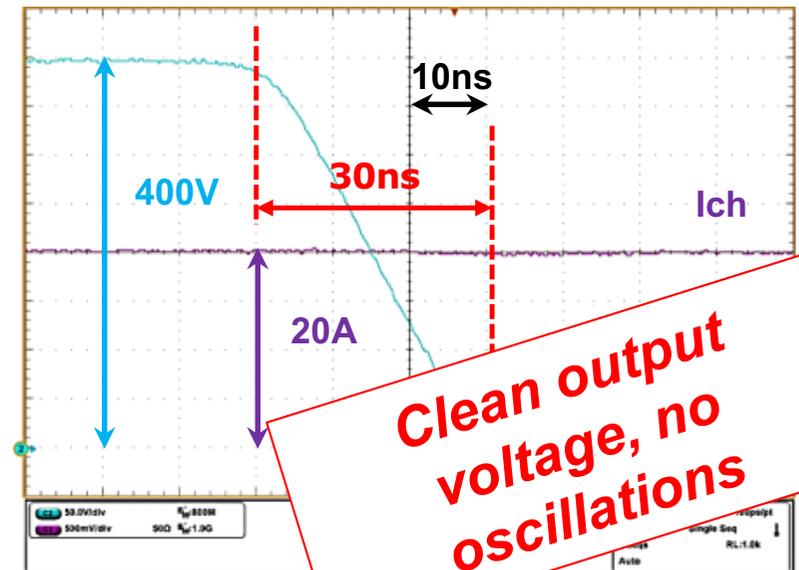
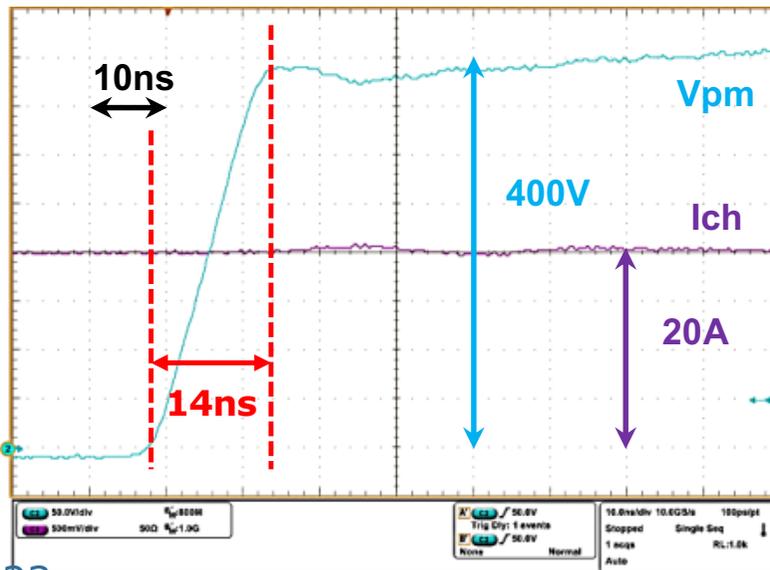
Kelvin source connection => Common source inductance negligible

Bus-bar design :

Low value of stray inductance
Very low mutual coupling between gate circuit and power circuit



INCA3D gate circuit model



Clean output voltage, no oscillations

PCOC Module: conclusion

- New high speed GaN and SiC devices necessitate dedicated packaging, both on power and gate part to express their performances. Package parasitics generates voltage overshoot, ringing, EMI
- Parasitics have to be carefully managed. Stray interactions have to be used in a positive way. Shielding help also to reduce EMI.
- Complexity of managing parasitics, the future of High speed Power Electronics is integration:
 - Decoupling cap, driver, EMC filter (layout) in the package, all optimized once for all
 - Reliability, cost, recycling and sustainability issues: ***packaging is not only electromagnetism***



Merci pour votre attention

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