



Automatic Design Tool for PCB Embedded technology

Editor: Bahaeddine BEN HAMED

**Thesis Managers: Cyril BUTTAY
Guillaume REGNAT
Guillaume LEFEVRE**

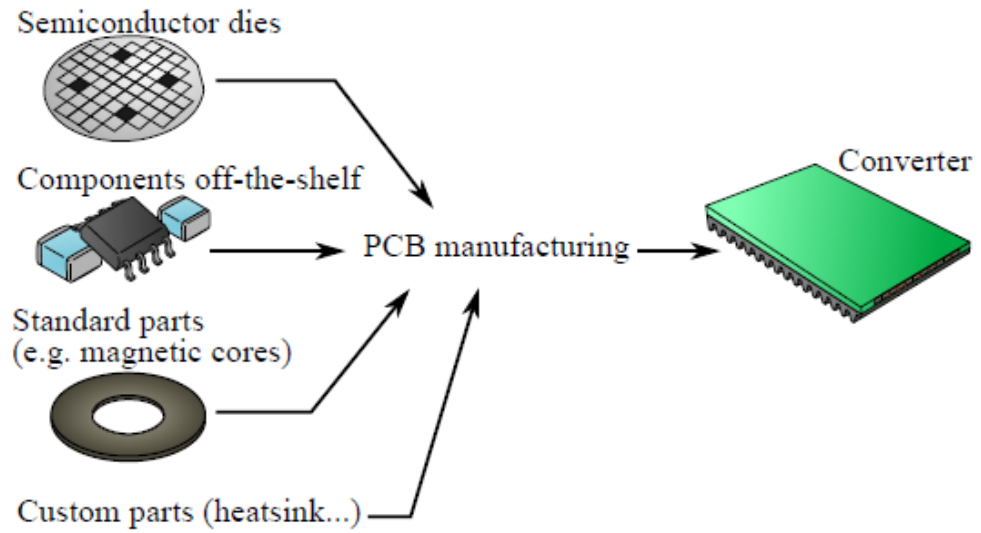
02/02/2023

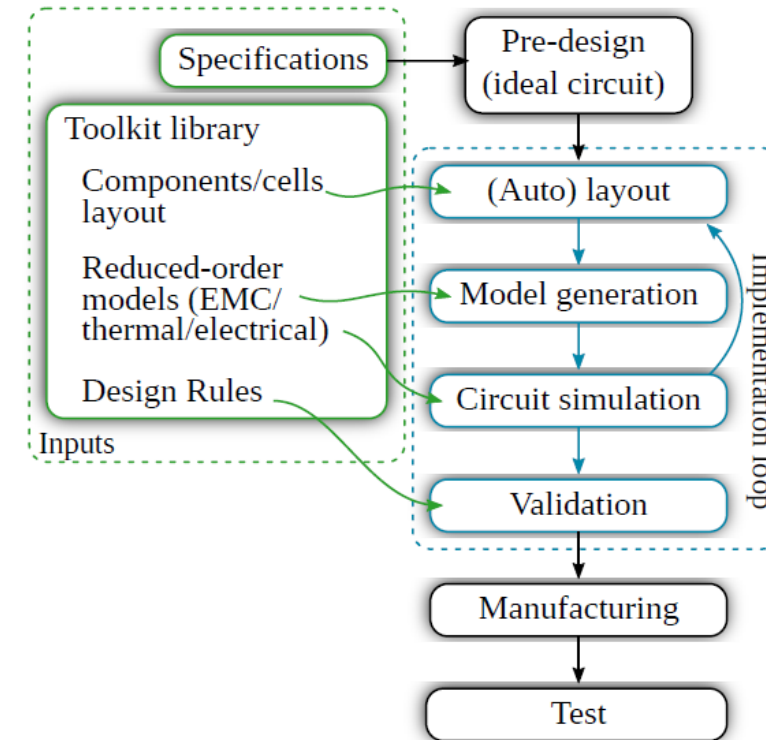
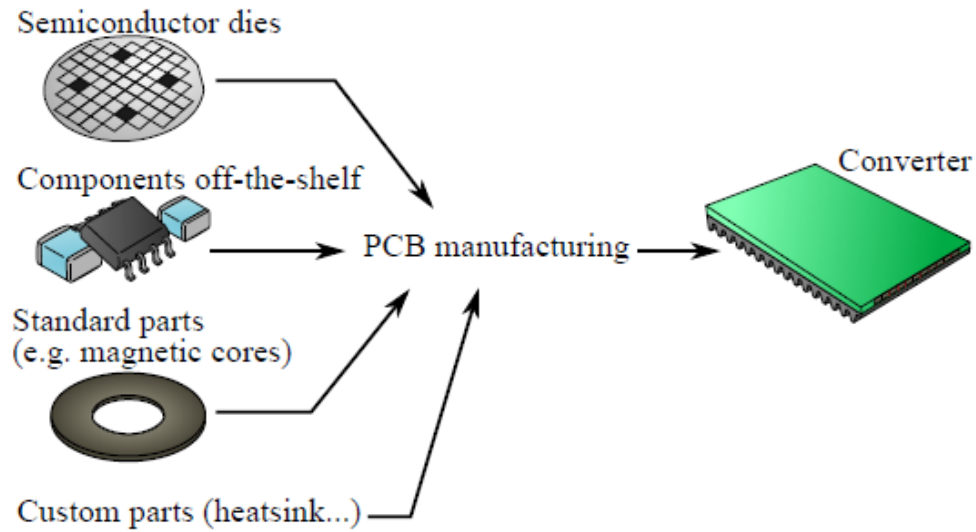
MITSUBISHI ELECTRIC R&D CENTRE EUROPE

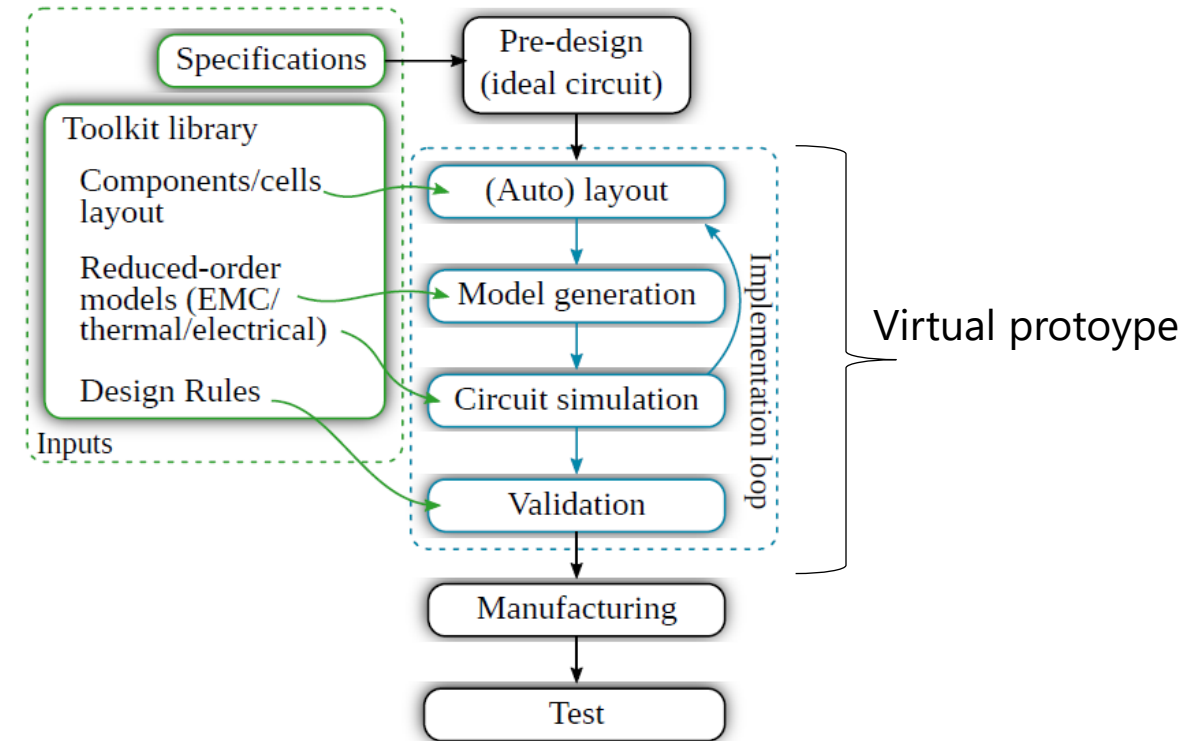
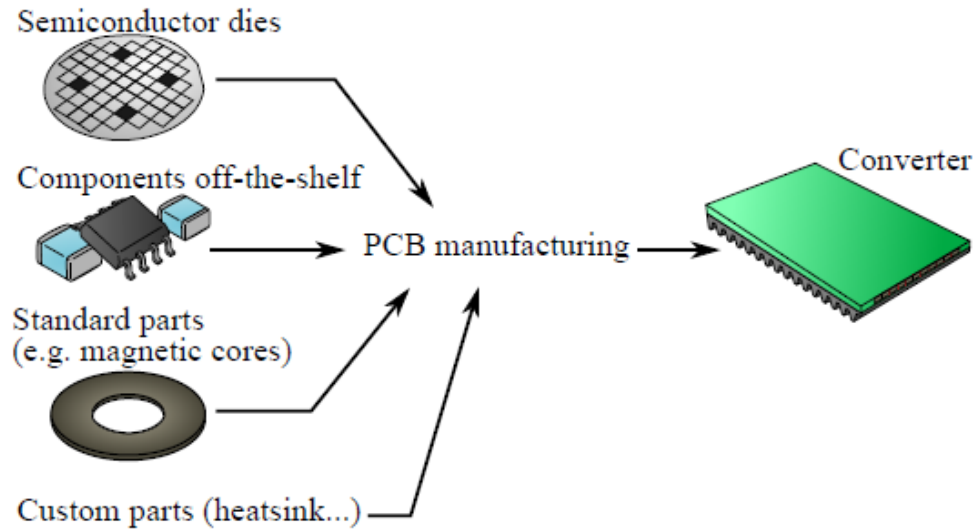
1

Introduction

Automatic Design Tool for PCB Embedded technology

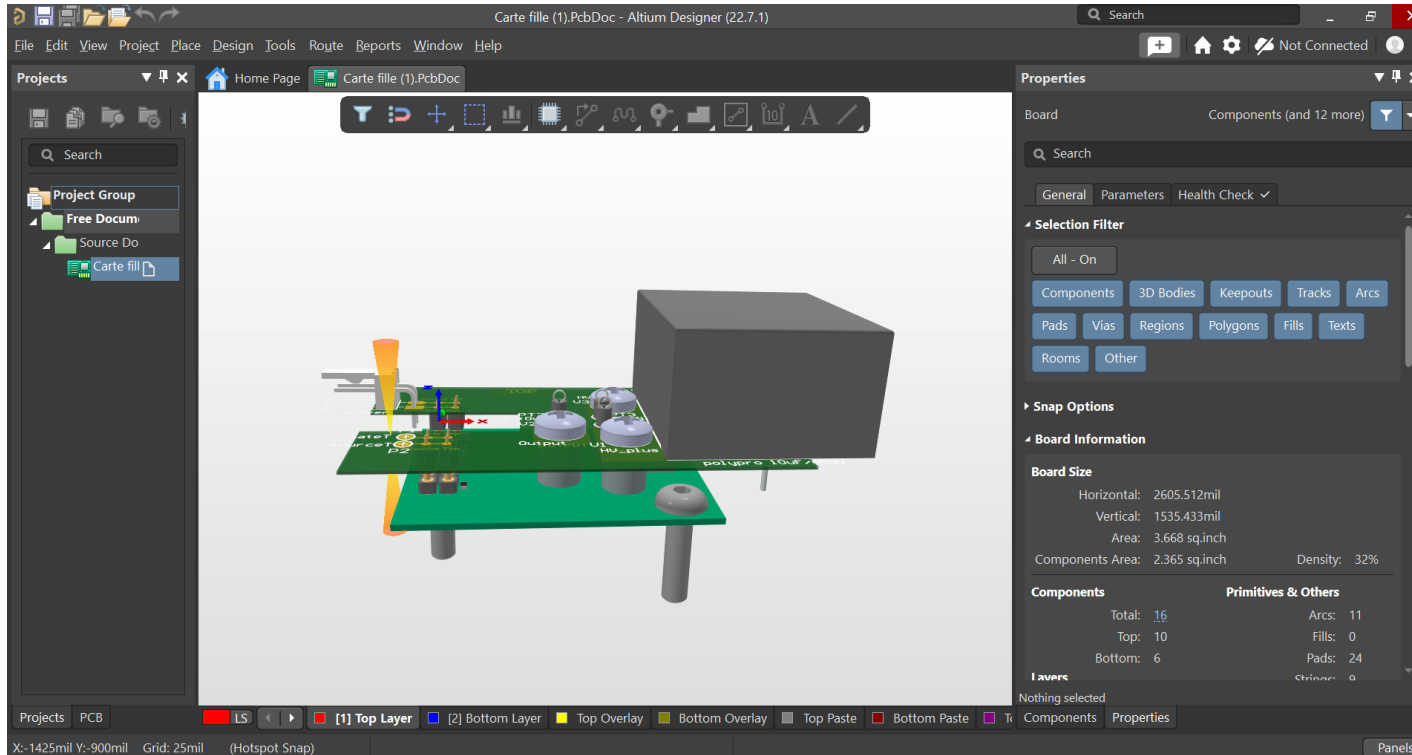






eCAD

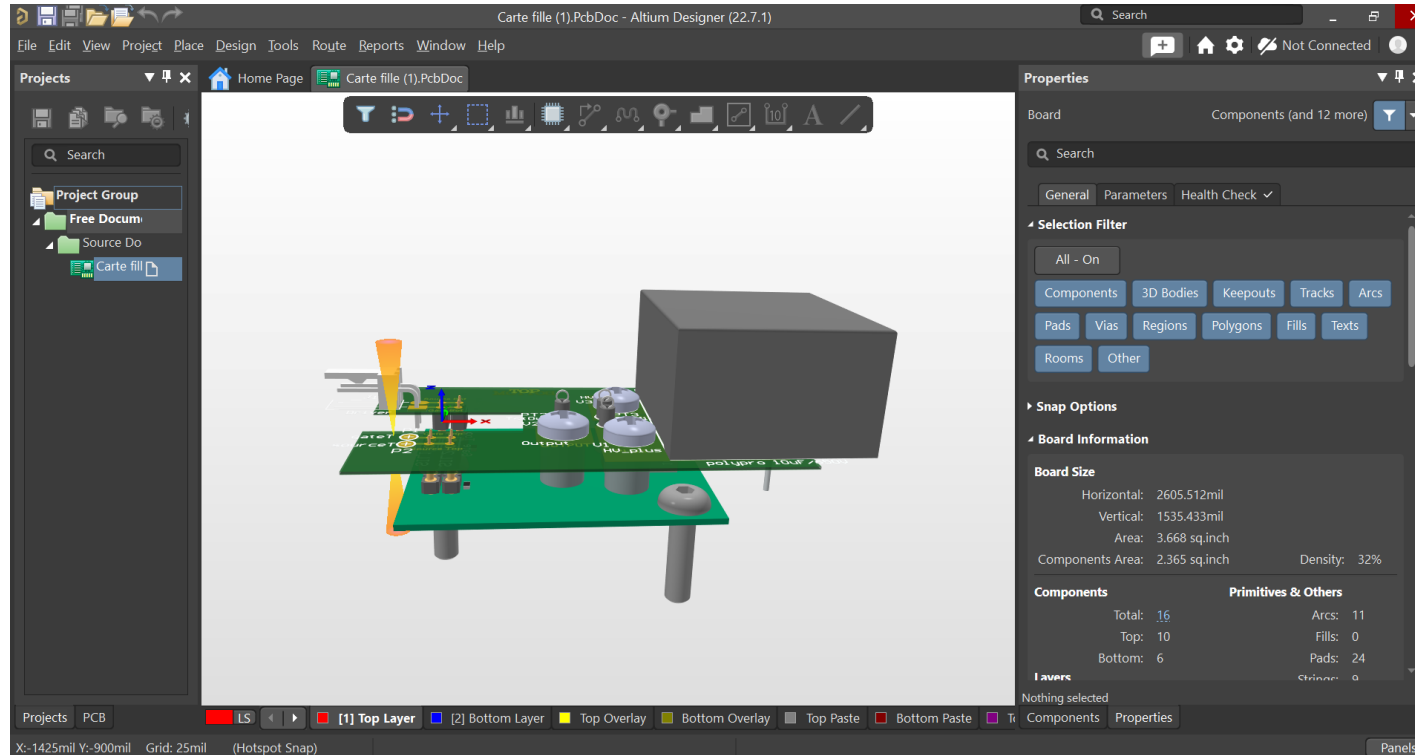
The entire structure of a PCB-embedded converter is described in the eCAD tool



- Layout
 - Layers materials
 - Layers dimensions
- Components:
 - pins info
 - Location
 - Value
- And more : schematic ...

eCAD

The entire structure of a PCB-embedded converter is described in the eCAD tool



- Layout
 - Layers materials
 - Layers dimensions
- Components:
 - pins info
 - Location
 - Value
- And more : schematic ...

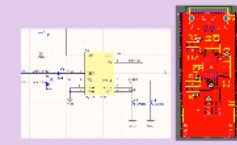
Is-it possible to generate a virtual prototype from this description ?

Generate a virtual prototype from the detailed circuit description available in the PCB CAD:

- Simulation of the complete PCB model (**thermal**, electrical & **coupled models**)
- Use of existing modelling software

Design Toolkit

PCB Layout
Altium Designer



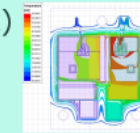
eCAD

C++

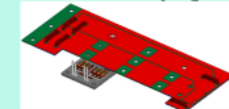
Finite element
simulation
(Ansys)

Vbscript

Thermal simulation
(icepak)

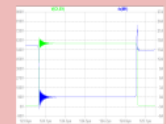
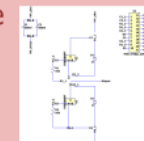


Circuit parasitics
calculation (Q3D)



Circuit
Simulation

Time-domain
simulation
(LTspice)



Generate a virtual prototype from the detailed circuit description available in the PCB CAD:

- Simulation of the complete PCB model (**thermal**, electrical & **coupled models**)
- Use of existing modelling software

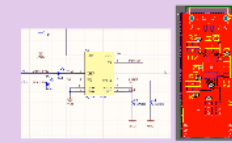
Electrical modelling approach realized:

- Generate a readable LTspice schematic which includes the parasitic effect of the interconnections
→ Validation of the electrical behavior

Design Toolkit

PCB Layout

Altium Designer

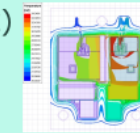
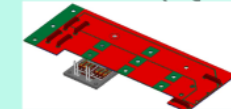
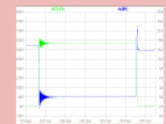
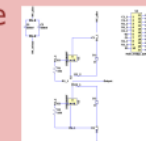


eCAD

C++

Finite element
simulation
(Ansys)

Vbscript

Thermal simulation
(icepak)Circuit parasitics
calculation (Q3D)Circuit
SimulationTime-domain
simulation
(LTspice)

Generate a virtual prototype from the detailed circuit description available in the PCB CAD:

- Simulation of the complete PCB model (**thermal**, electrical & **coupled models**)
- Use of existing modelling software

Electrical modelling approach realized:

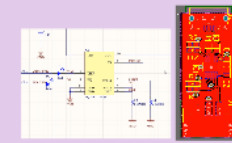
- Generate a readable LTspice schematic which includes the parasitic effect of the interconnections
→ Validation of the electrical behavior

Thermal modelling approach in progress

- Generate a reduced-order thermal model (RC-network equivalent thermal model)
- Add the RC-network to the LTspice schematic
→ Validation of the thermal behavior

Design Toolkit

PCB Layout
Altium Designer



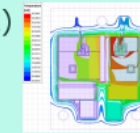
eCAD

C++

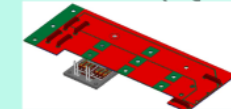
Finite element
simulation
(Ansys)

Vbscript

Thermal simulation
(icepak)

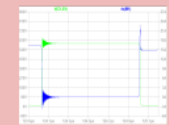
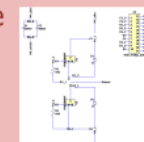


Circuit parasitics
calculation (Q3D)



Circuit
Simulation

Time-domain
simulation
(LTspice)

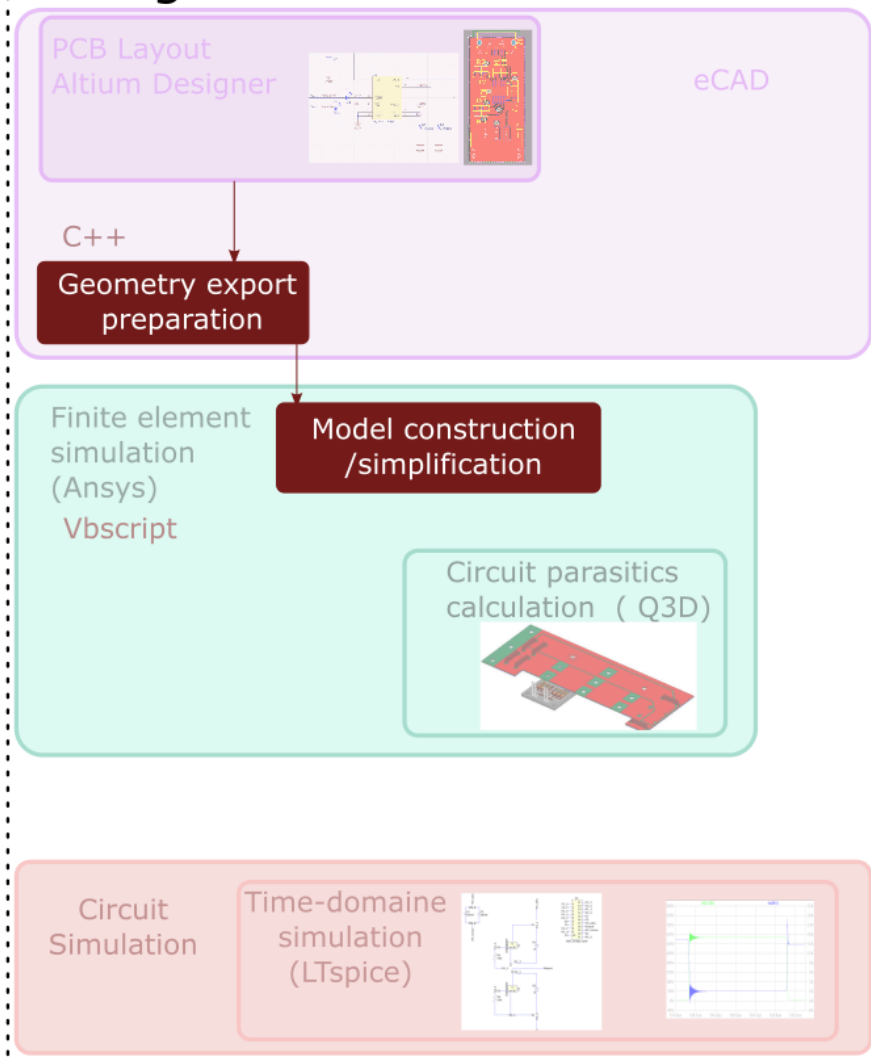


2

Electrical modelling

Automatic Design Tool for PCB Embedded technology

Design Toolkit



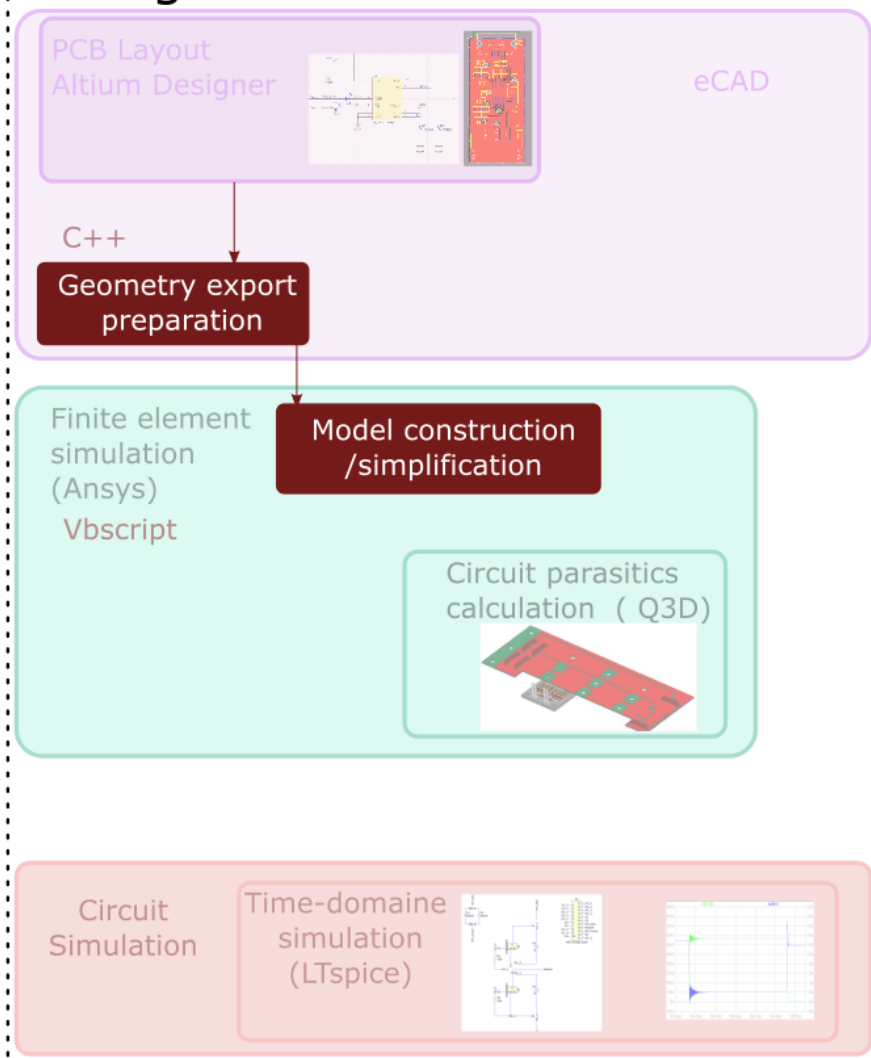
Data Export format

Many file format are available

Importing data in Ansys :

| | Gerber | ODB++ | IPC-2581 | EDB |
|-------------------------------------|--------|-------|----------|-----|
| 3D-model | -- | - | - | ++ |
| Layout details (materials, Nets) | -- | - | + | ++ |
| Components details | -- | - | + | ++ |

Design Toolkit



Data Export format

Many file format are available

Importing data in Ansys :

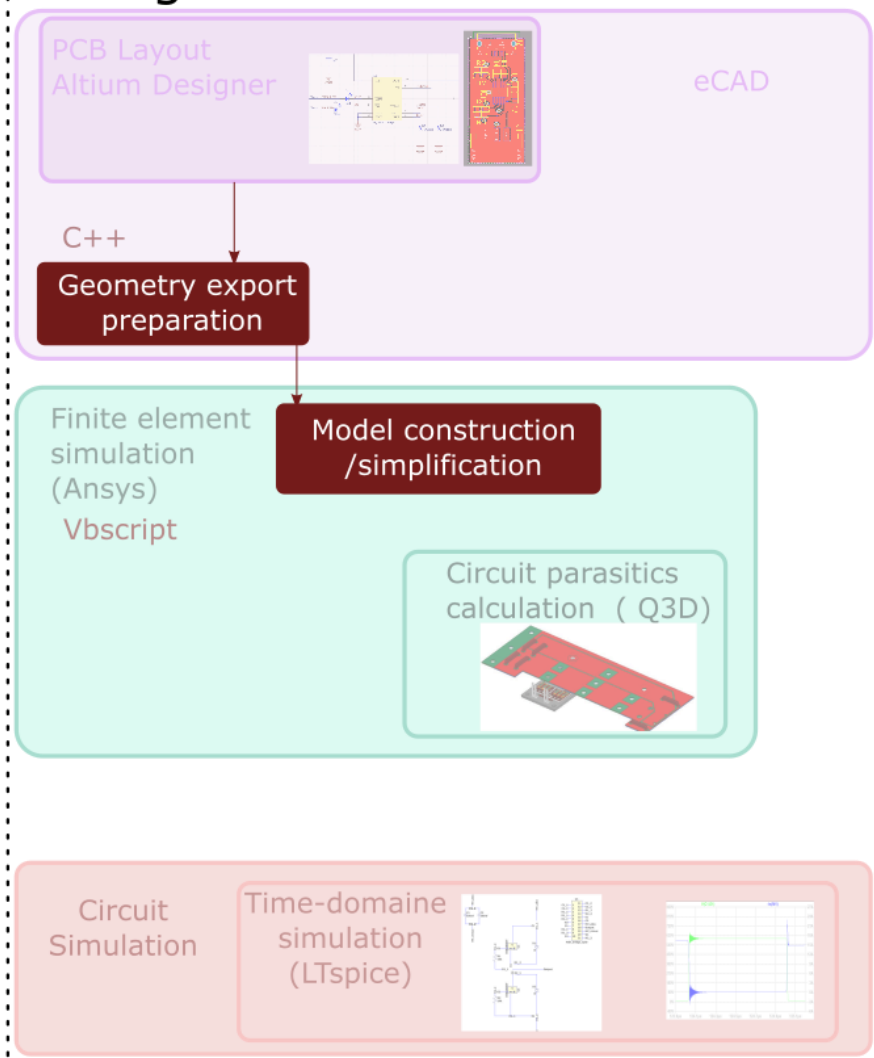
| | Gerber | ODB++ | IPC-2581 | EDB |
|----------------------------------|--------|-------|----------|-----|
| 3D-model | -- | - | - | ++ |
| Layout details (materials, Nets) | -- | - | + | ++ |
| Components details | -- | - | + | ++ |



Additional data required :

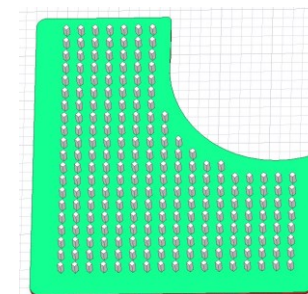
- Connection pads to be considered
- Via simplification data
- Some testbench info (e.g., Heatsink description)

Design Toolkit

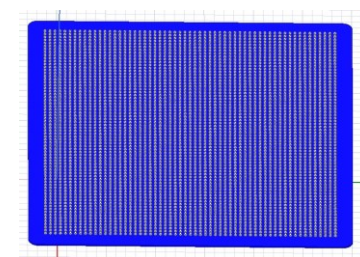


1. Geometry import
2. Simplify the geometry

- Faceting of round shapes (feature of Ansys)
- Grouping of vias

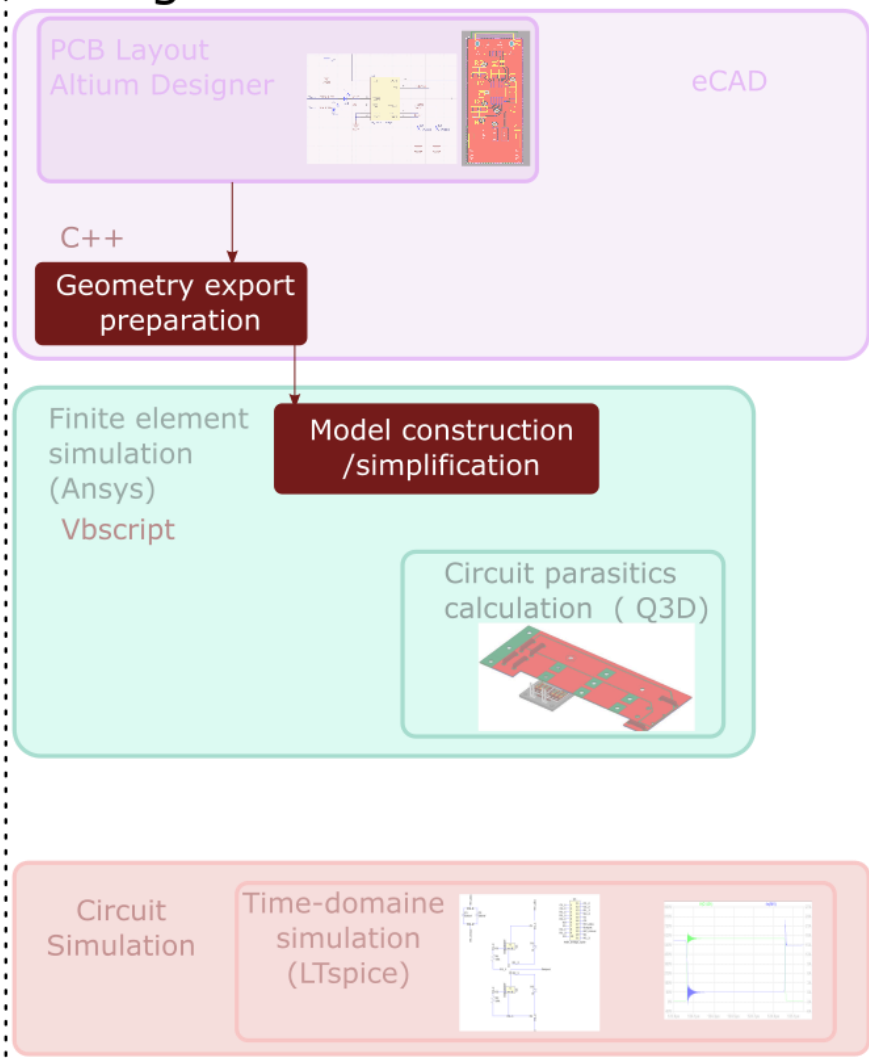


232 Via
Area= 10,44 mm²



4012 μ Via
Area=33,9014 mm²

Design Toolkit



1. Geometry import
2. Simplify the geometry

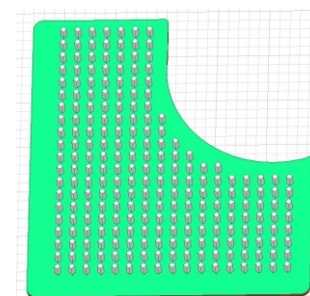
- Faceting of round shapes (feature of Ansys)
- Grouping of vias

Aims to reduce :

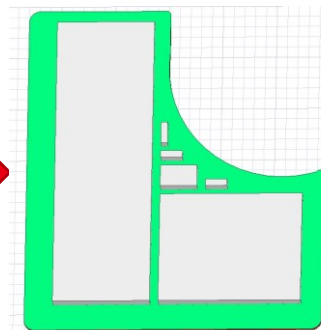
- the number of objects
- the complexity of the mesh

Limit the processing
time
&
memory

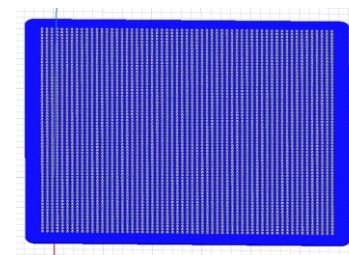
Simplification



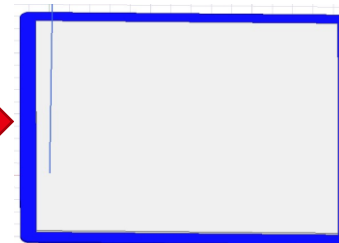
232 Via
Area= 10,44 mm²



6 « Via » groups
Area= 98,12 mm²
Ratio= 0,1

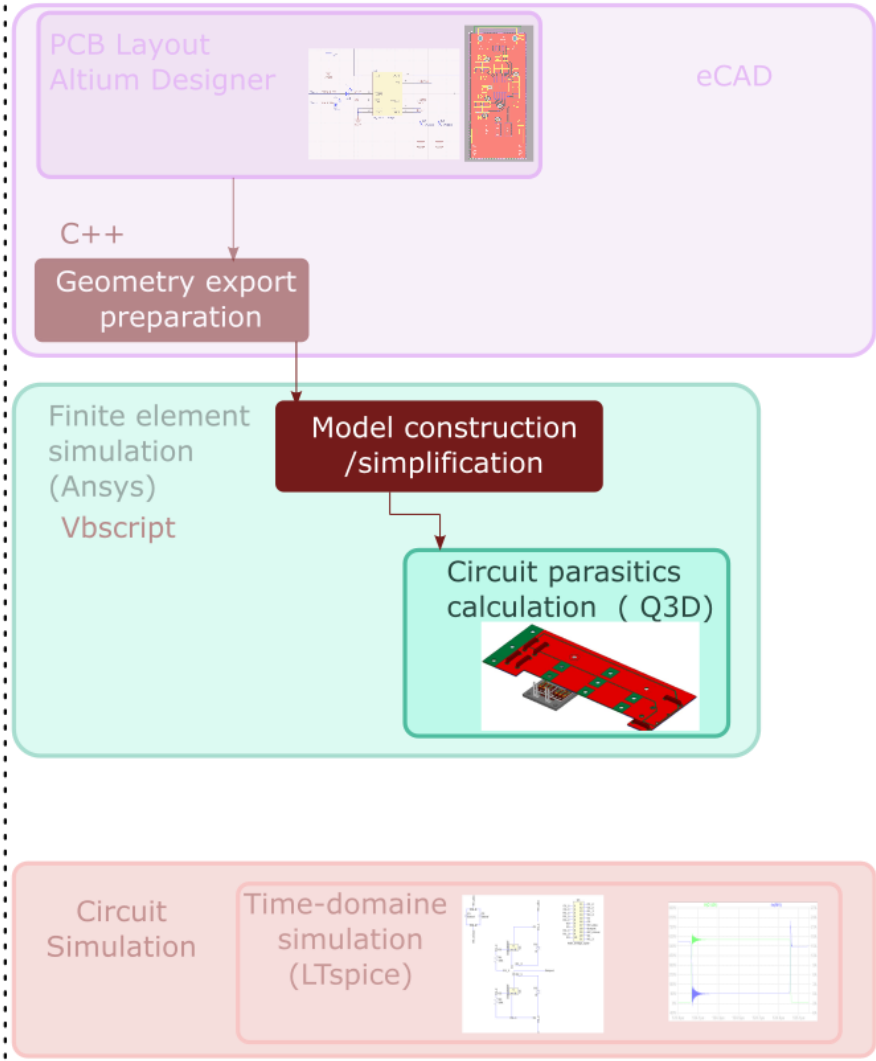


4012 μ Via
Area=33,9014 mm²



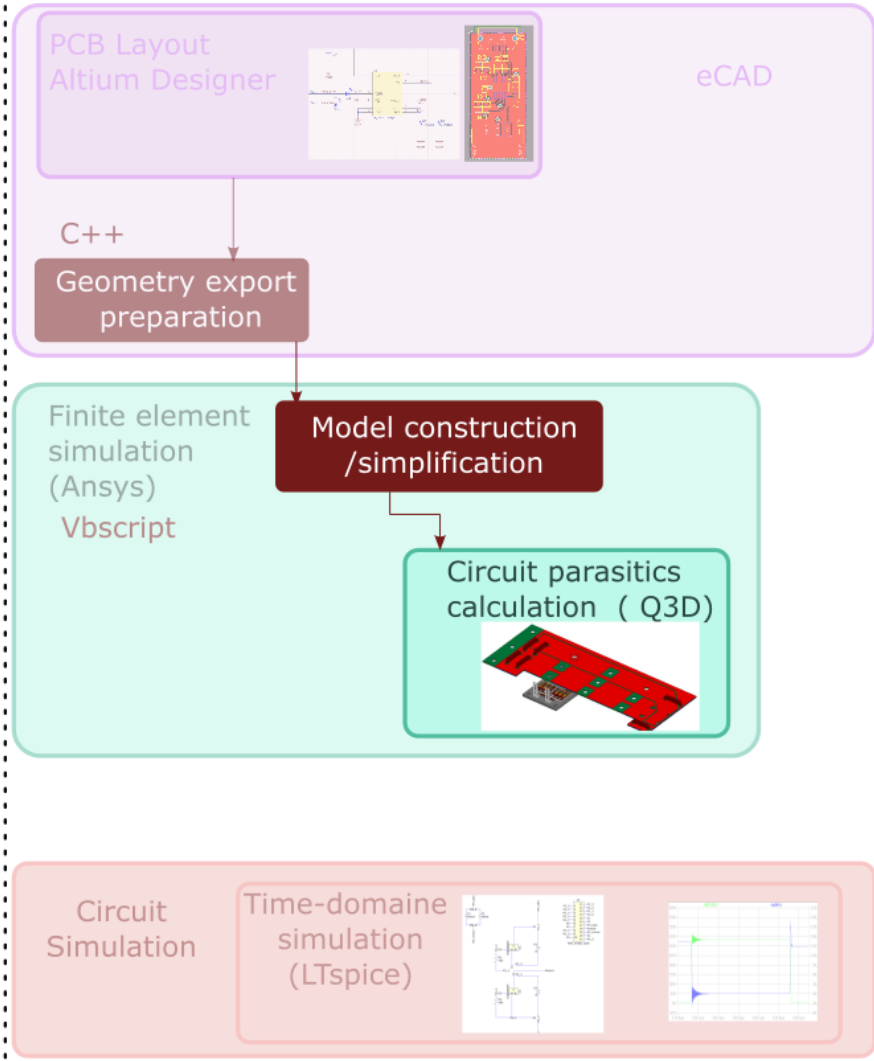
1 « Via » group
Area=254,853 mm²
Ratio =0,133

Design Toolkit



1. Geometry import
2. Simplify the geometry
3. Prepare the 3D-model for Q3D

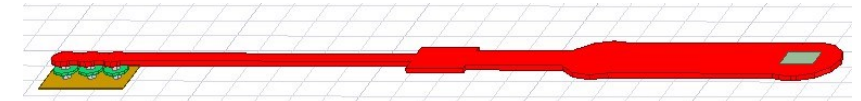
Design Toolkit



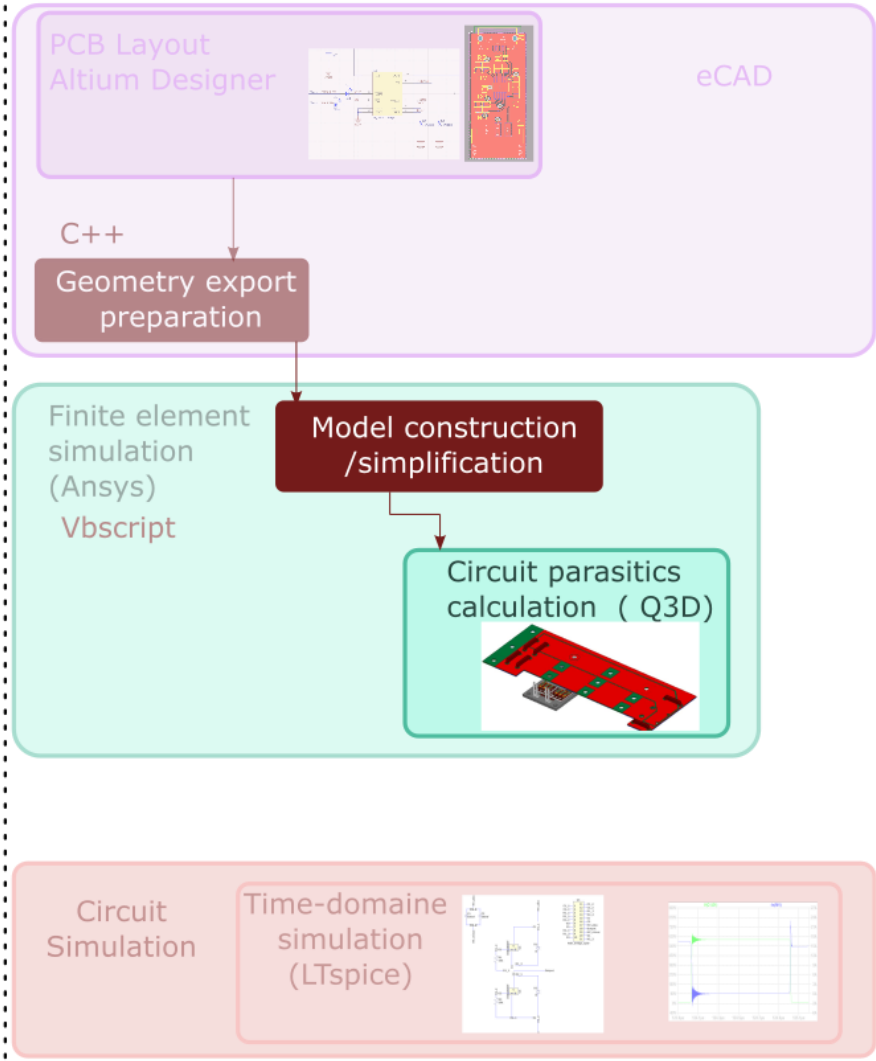
1. Geometry import
2. Simplify the geometry
3. Prepare the 3D-model for Q3D

- Automatic placement of the terminals (Sink/Source)

Net = connected conductors

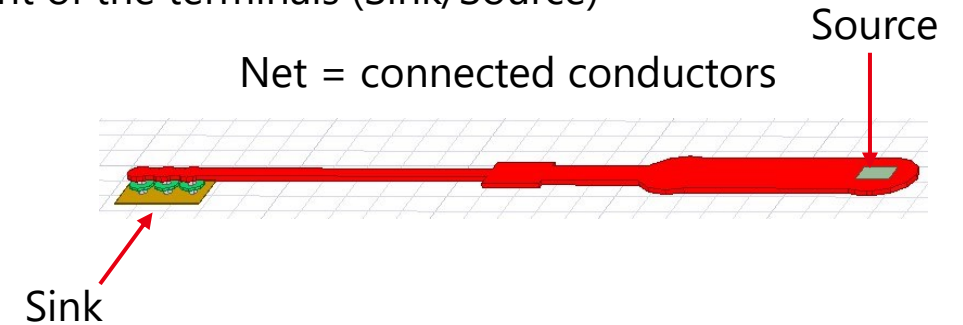


Design Toolkit

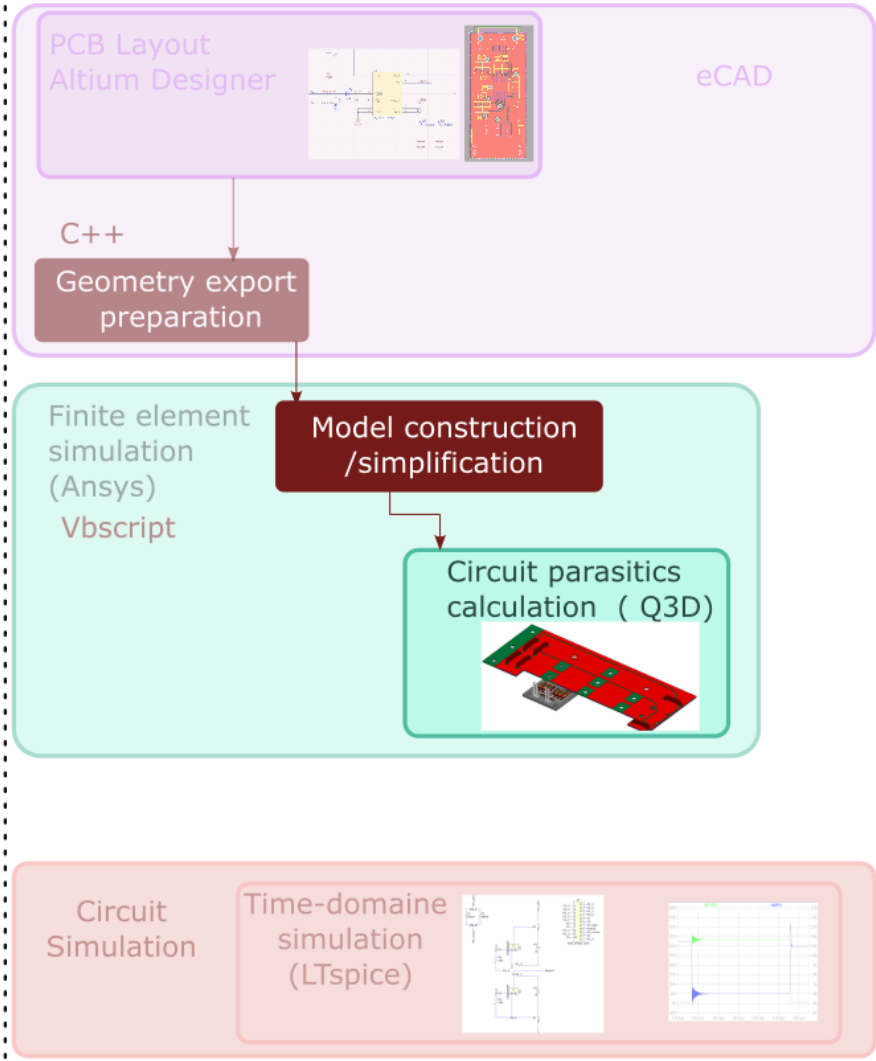


1. Geometry import
2. Simplify the geometry
3. Prepare the 3D-model for Q3D

- Automatic placement of the terminals (Sink/Source)

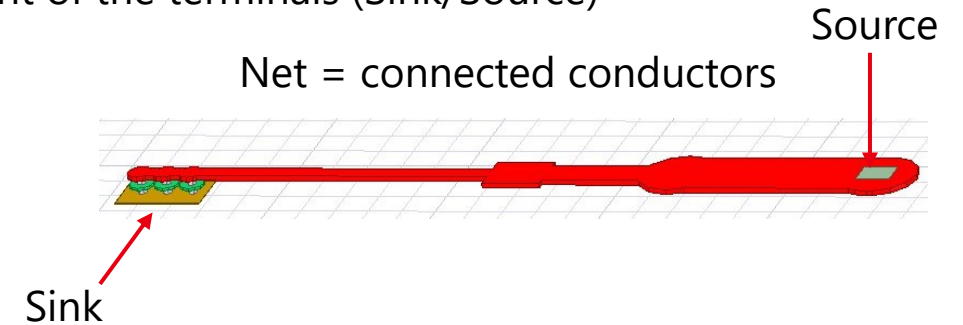


Design Toolkit

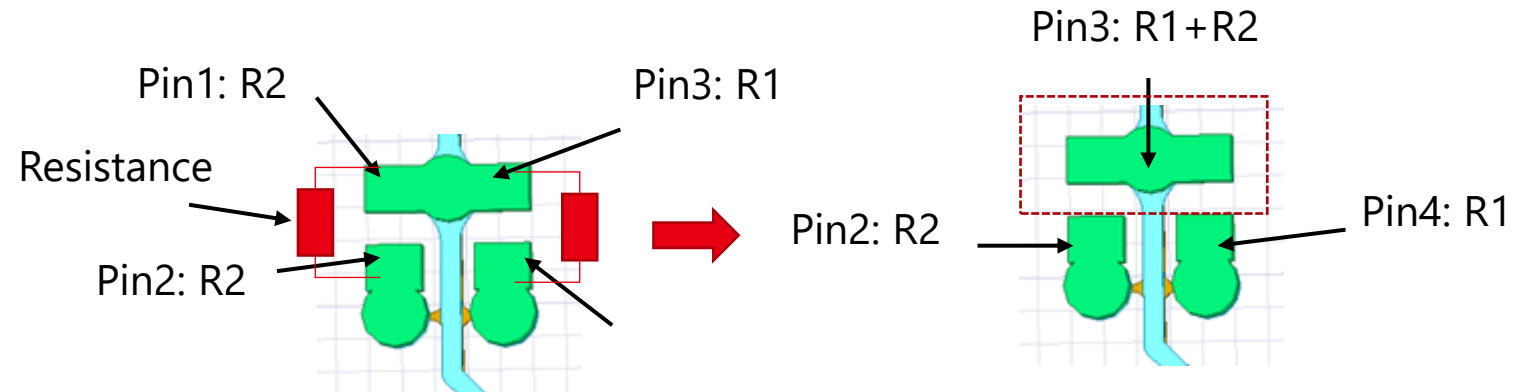


1. Geometry import
2. Simplify the geometry
3. Prepare the 3D-model for Q3D

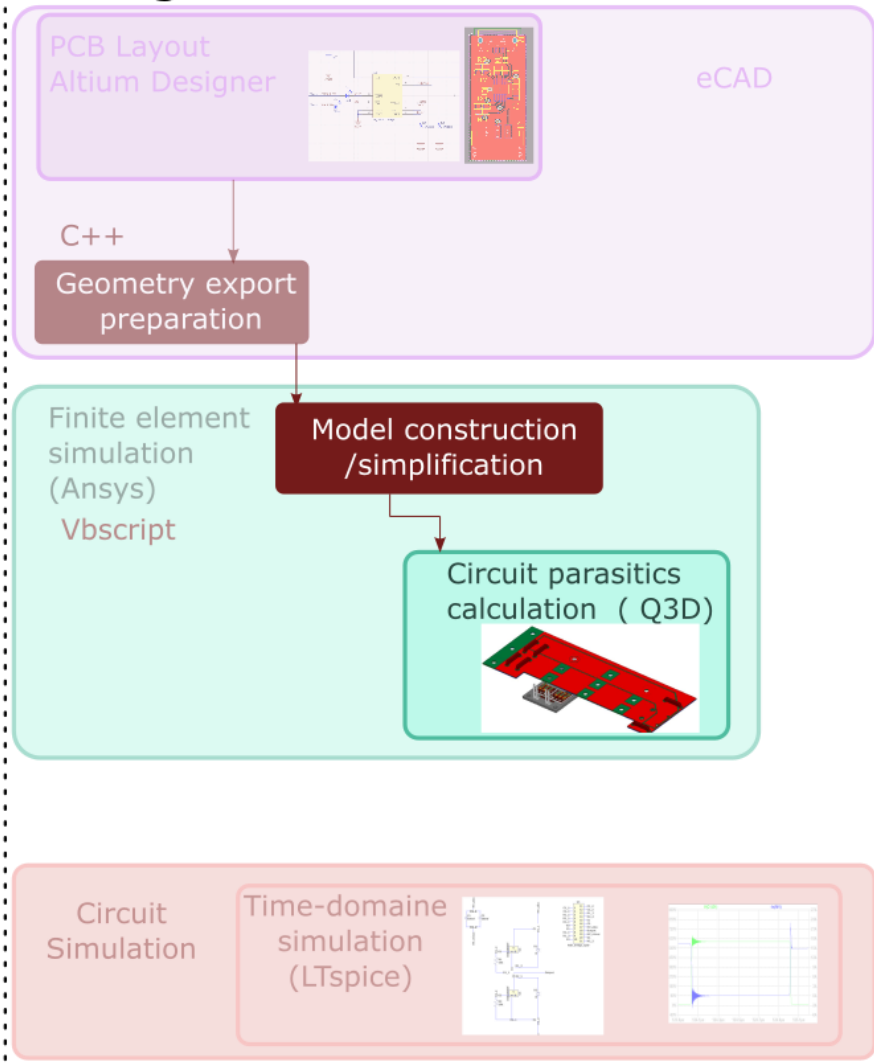
- Automatic placement of the terminals (Sink/Source)



- Terminals simplifications:

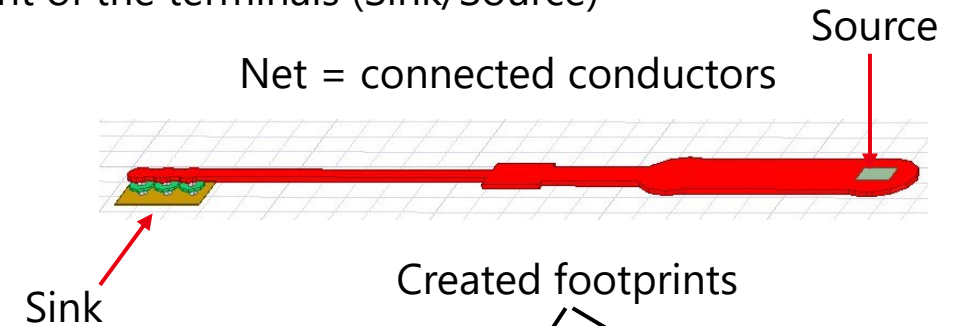


Design Toolkit

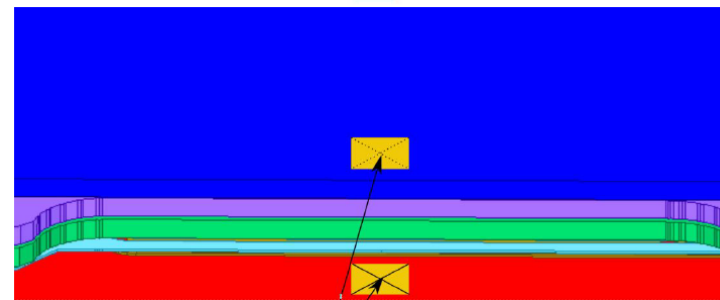


1. Geometry import
2. Simplify the geometry
3. Prepare the 3D-model for Q3D

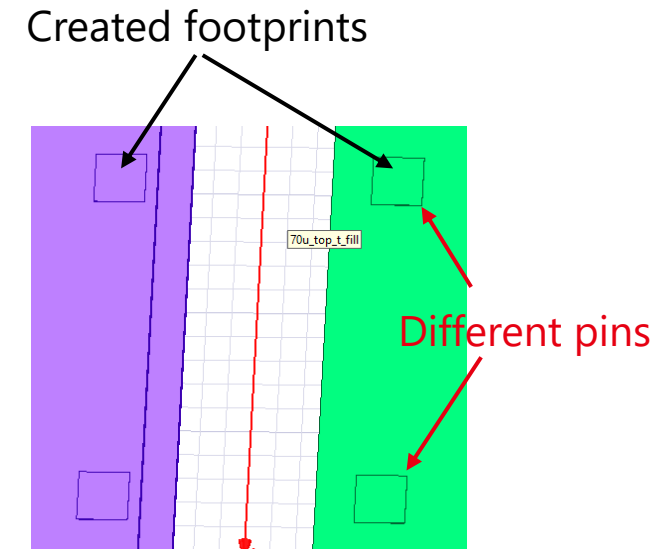
- Automatic placement of the terminals (Sink/Source)



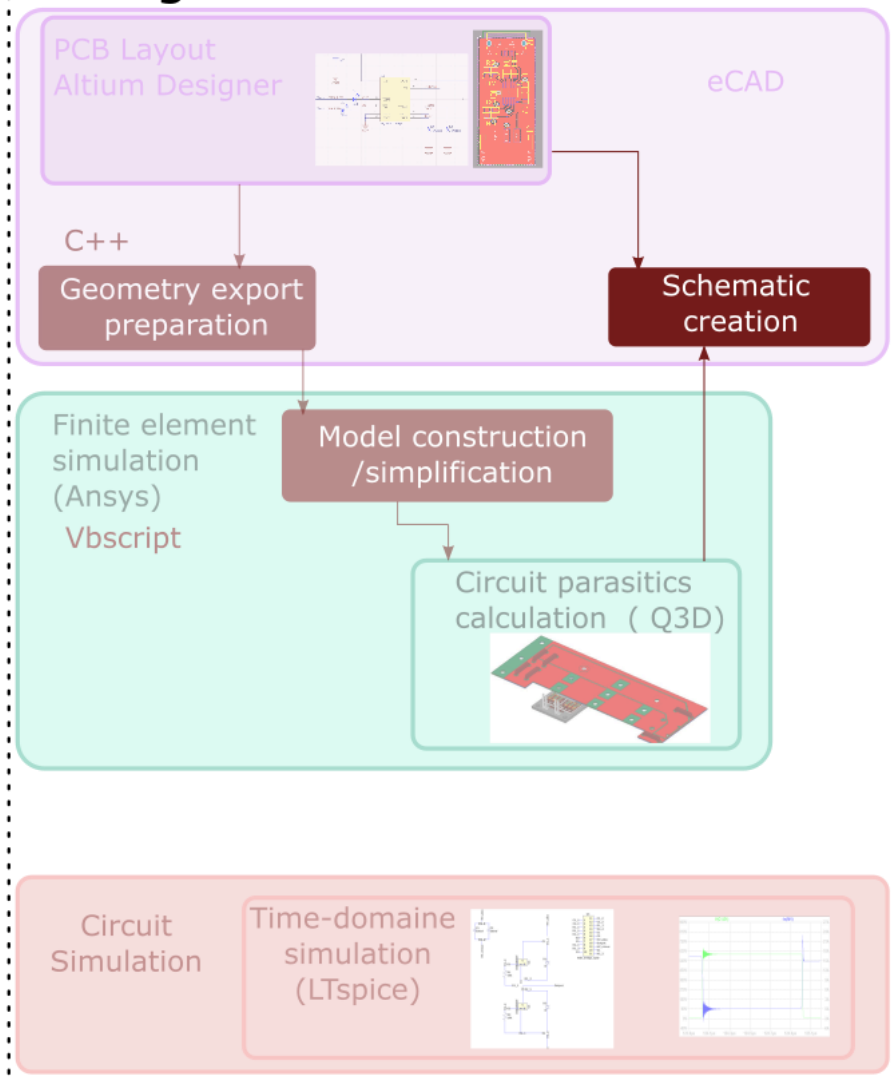
- Terminals simplifications:



Created footprints

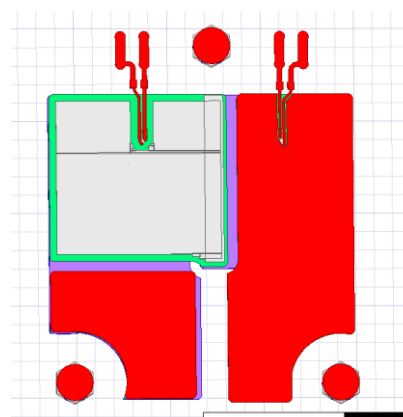


Design Toolkit



1. Geometry import
2. Simplify the geometry
3. Prepare the 3D-model for Q3D
4. Run stray R,L,C calculation between all terminals
5. Generate the SPICE model
6. Export the SPICE model terminals info to the custom extension (eCAD)

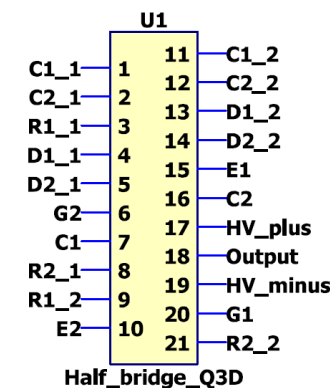
Ansys (Q3D 3D-Model)



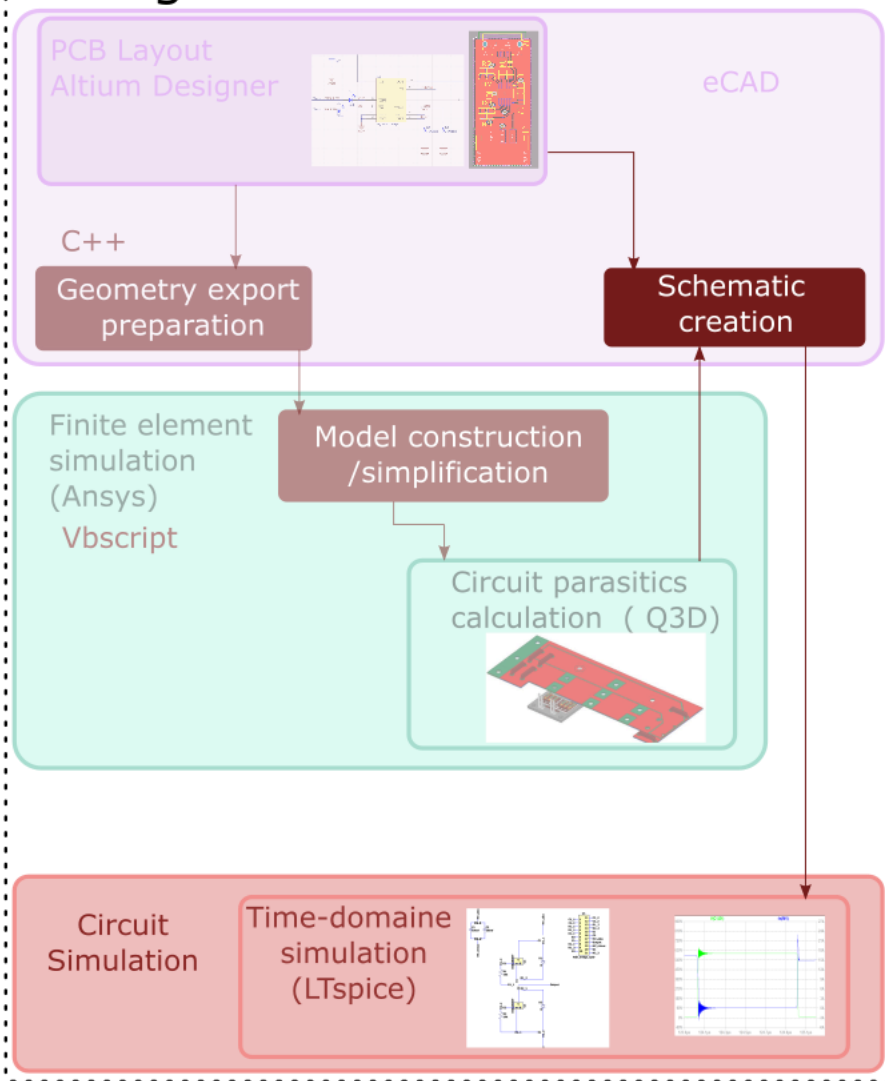
Number of VIAs : 103

Solved in ~ 4 min

Stray R,L,C equivalent circuit (LTspice)



Design Toolkit

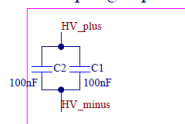


6. Export the SPICE model terminals info to the custom extension (eCAD)

7. Generate the complete LTspice schematic :

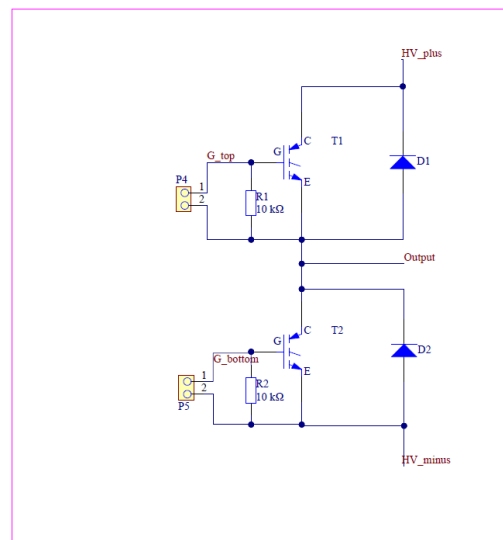
- Reproduce location of symbols (from Altium schematic)
- Layout model as single block
- Generate automatically the connections

Decoupling capacitor

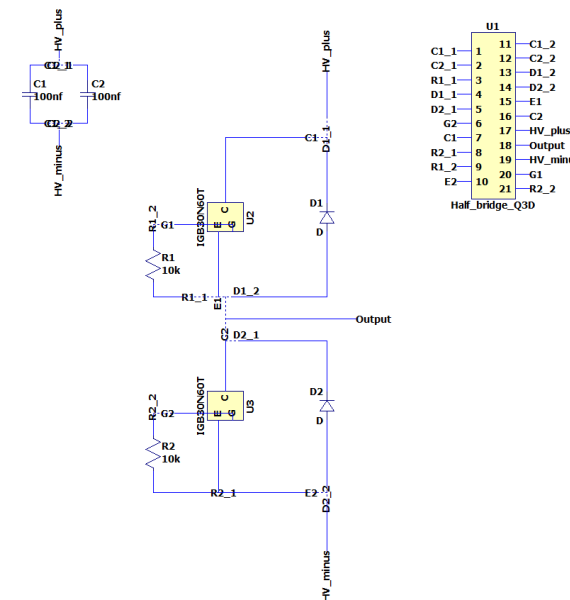


eCAD(Altium)

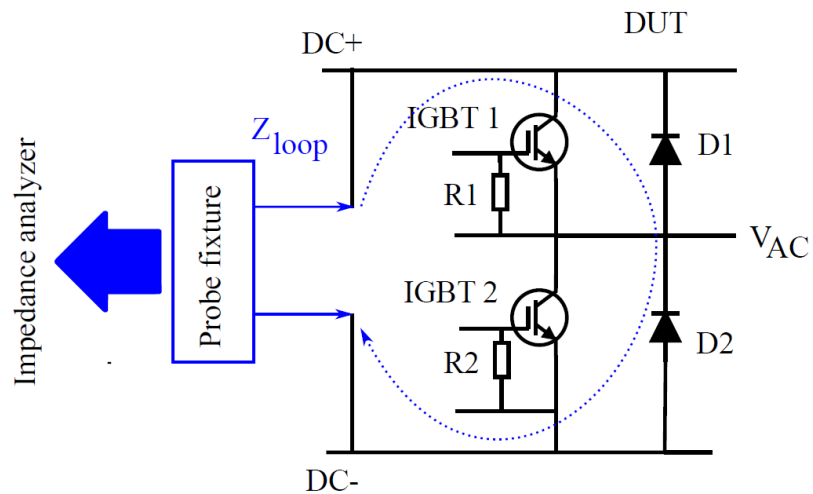
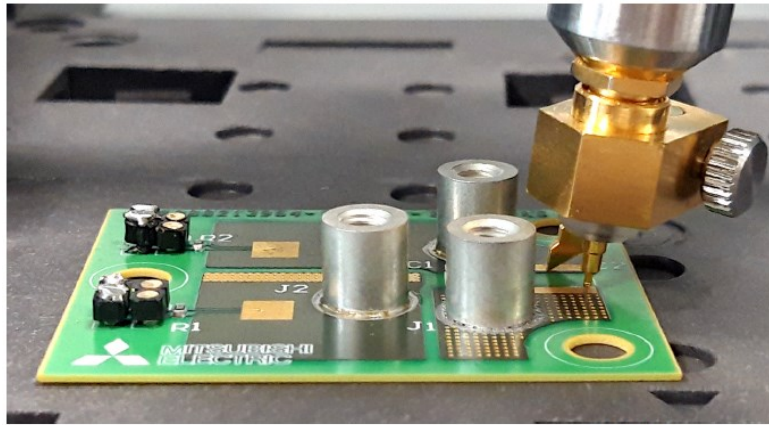
Power stage



Circuit simulation(LTspice)

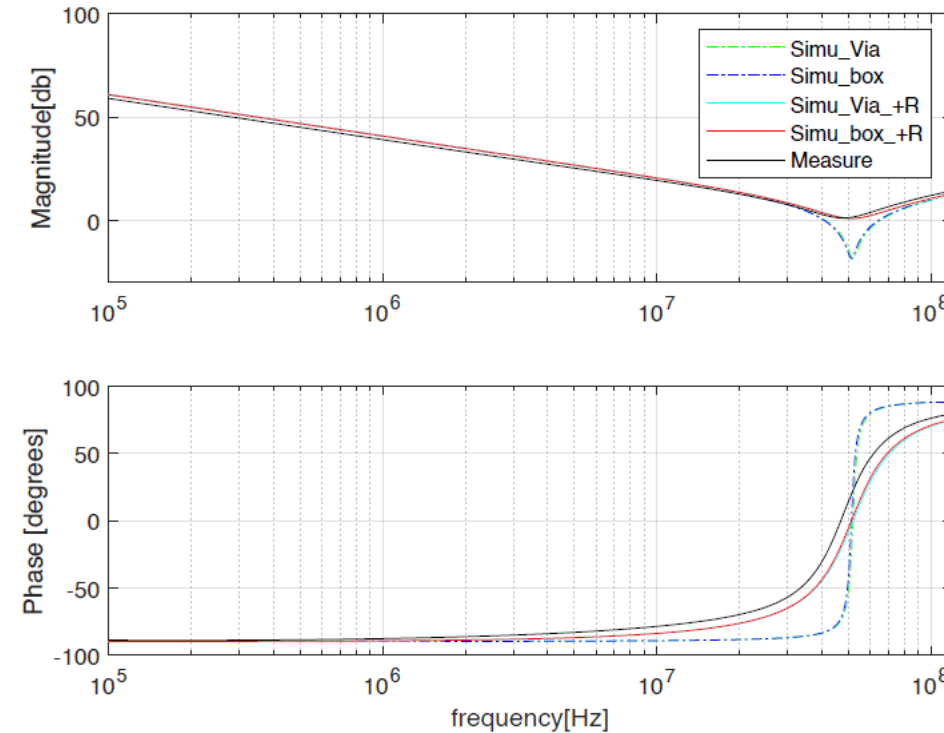


1. Characterization of circuit impedances



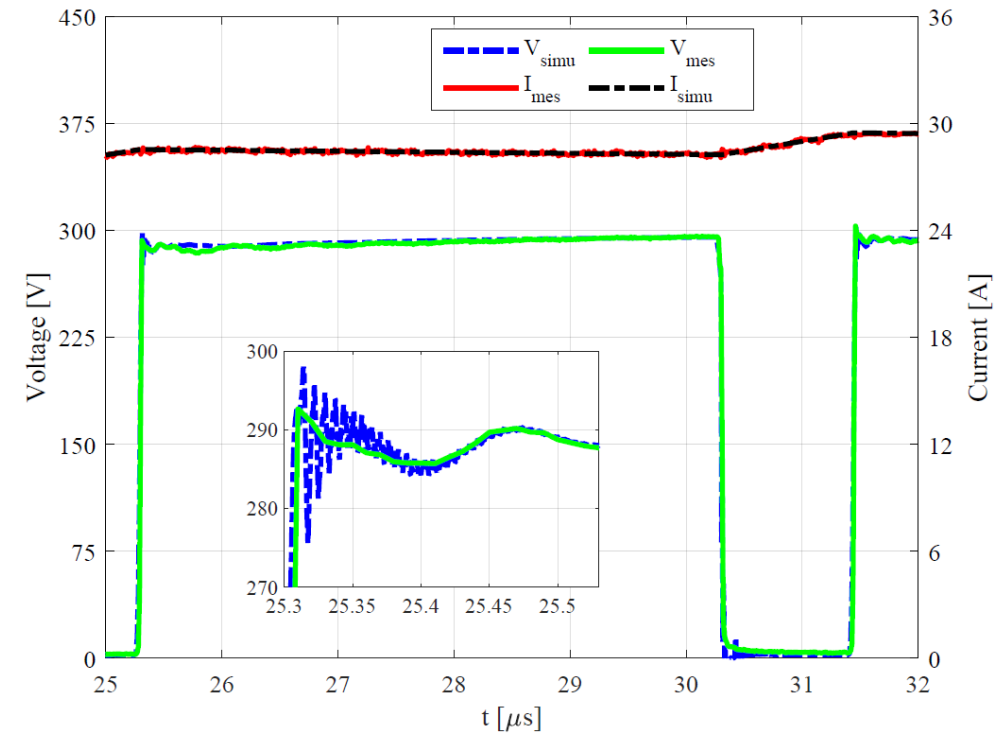
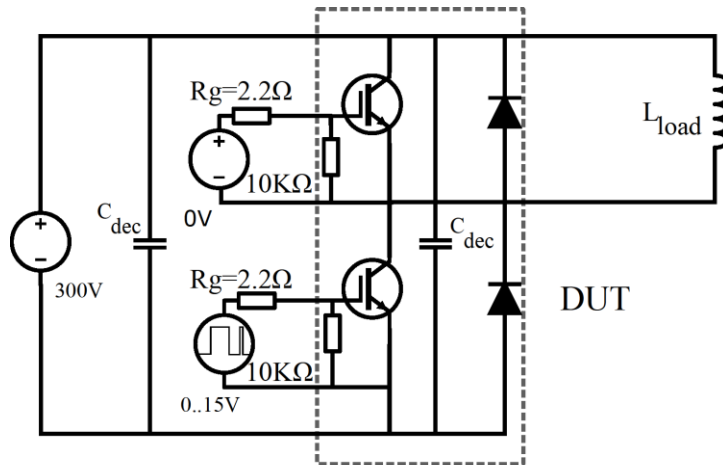
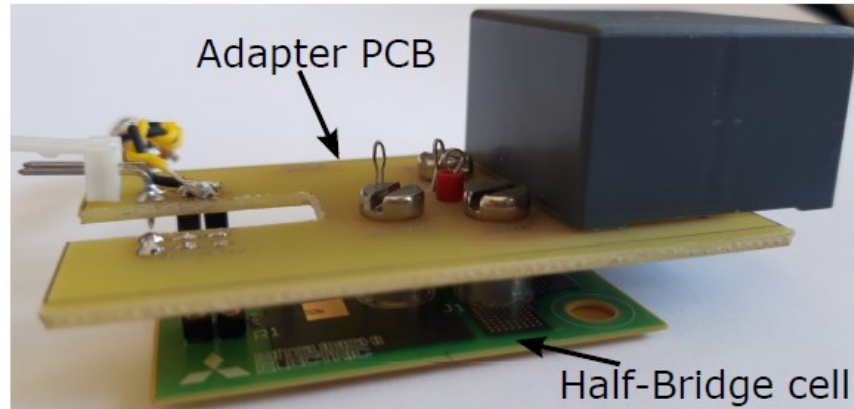
Impedance :

Simulation vs Measurement



- No bad effect of the of the geometry simplification
- Measurement accuracy limited (contact prob ...)
- Good simulation/experiment agreement overall

2. Double pulse test



- Used equivalent Spice model for the IGBT & Diode
- Good match between measurement & simulation



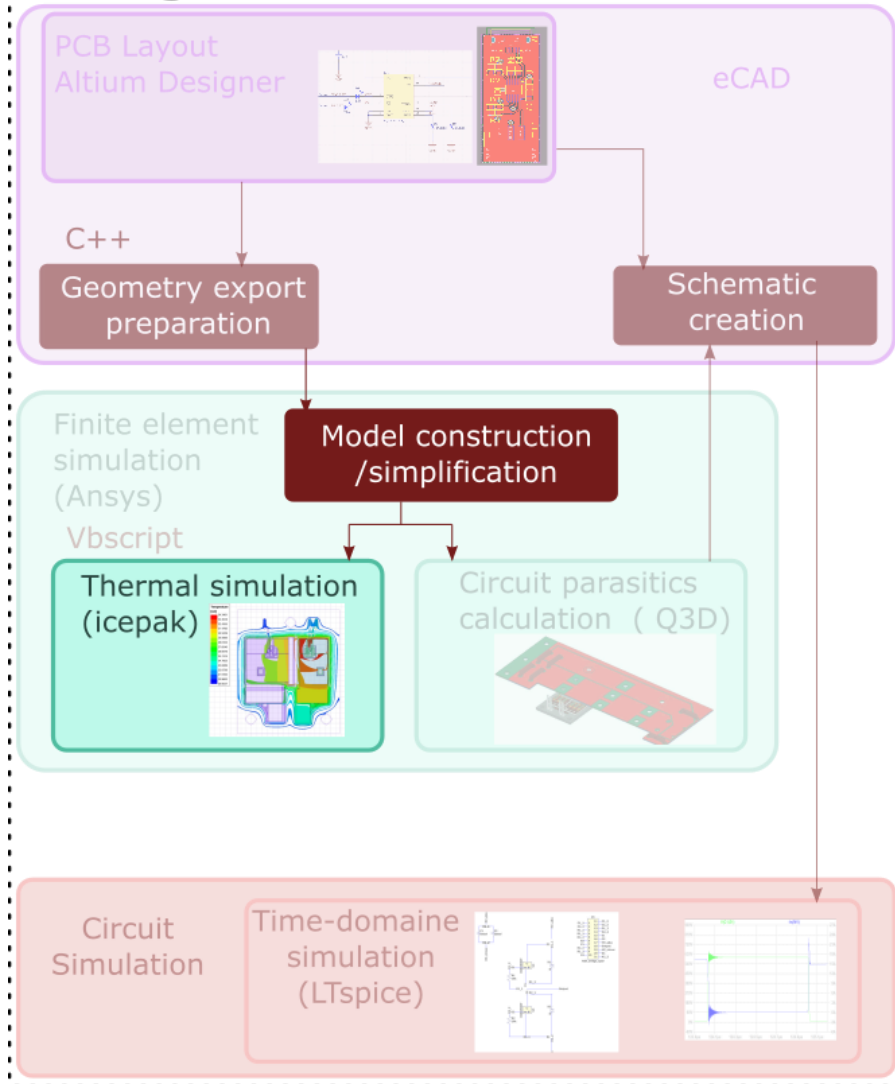
Results validate the electrical modelling approach

3

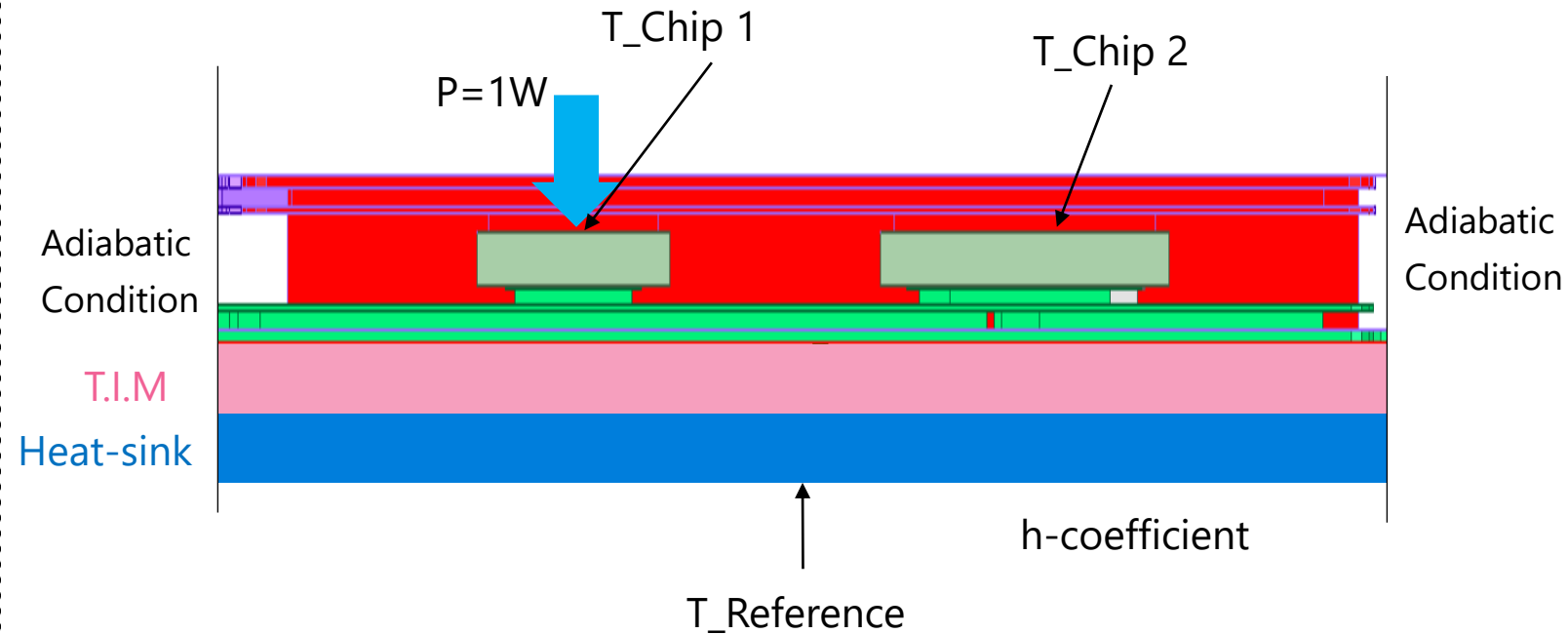
Thermal Modelling

Automatic Design Tool for PCB Embedded technology

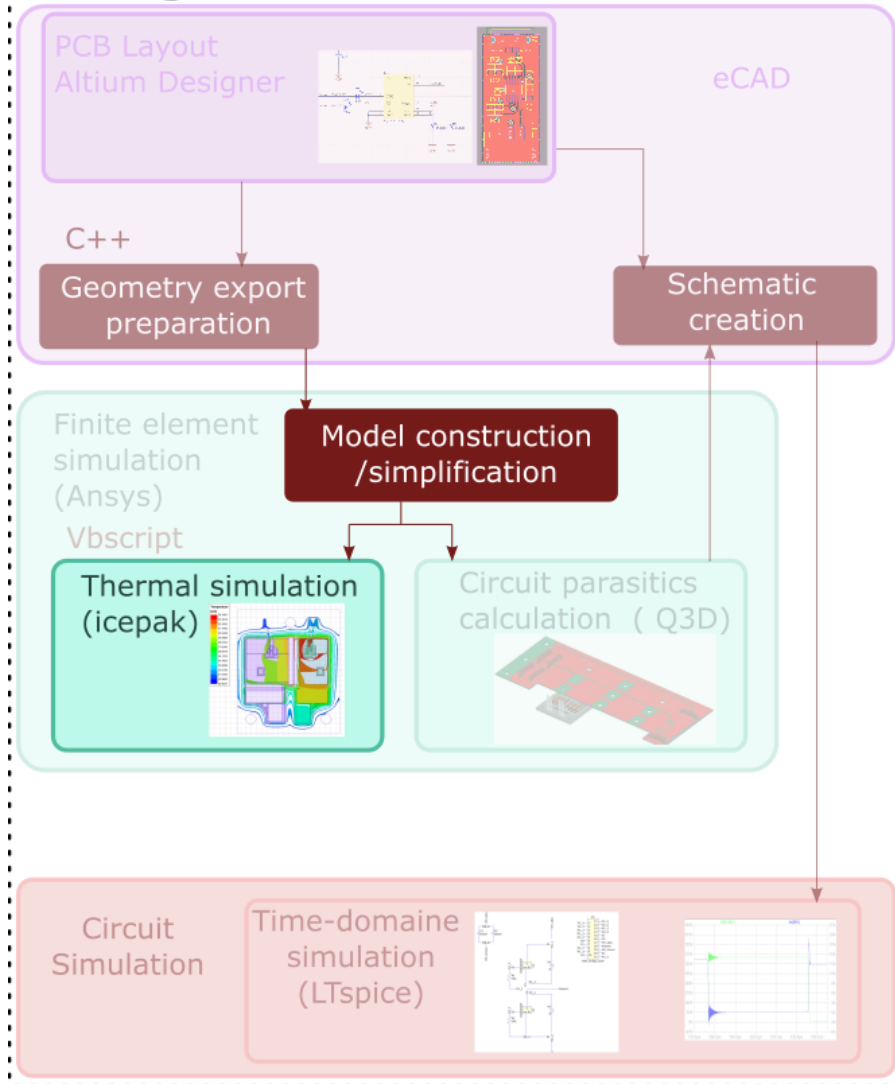
Design Toolkit



Run the thermal transient simulation

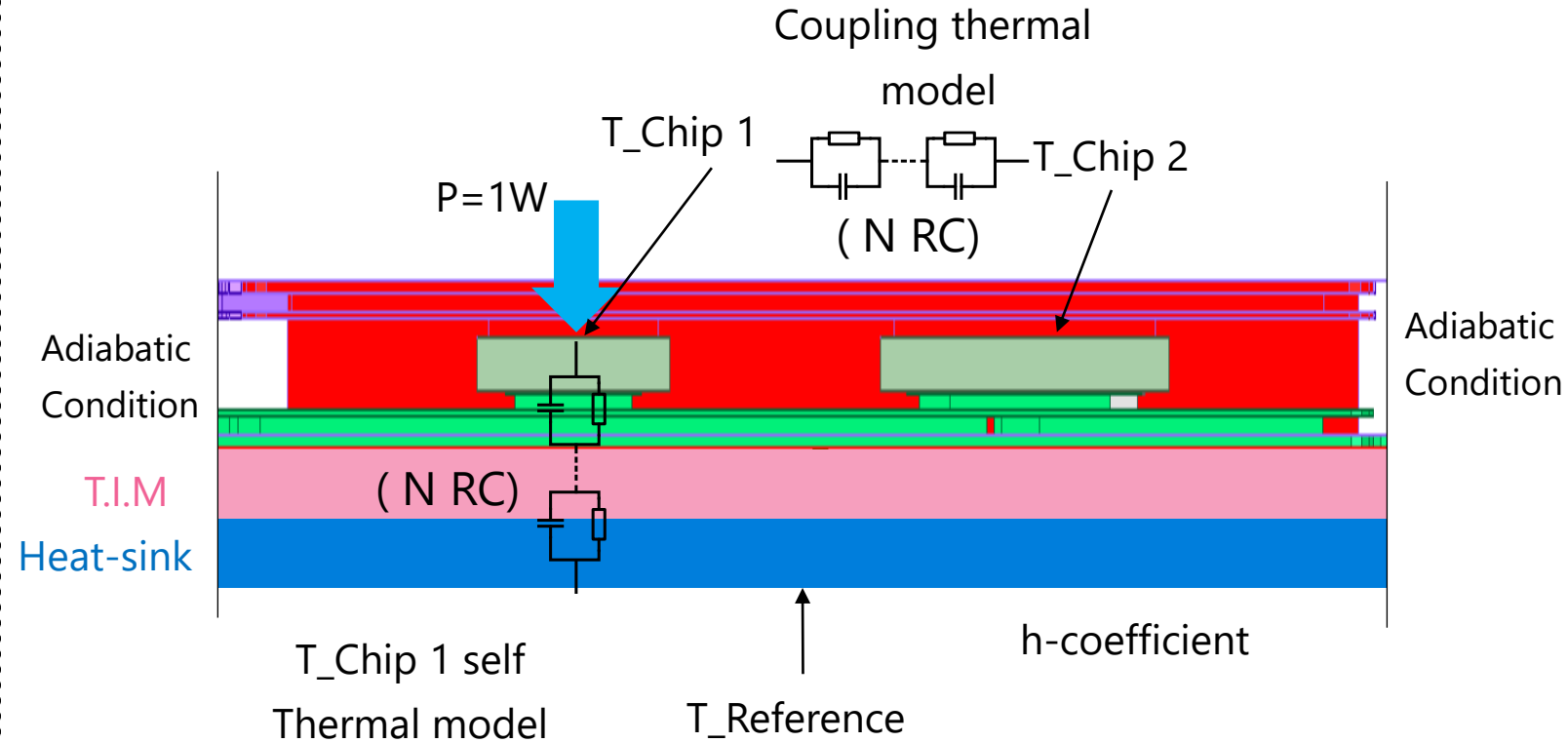


Design Toolkit

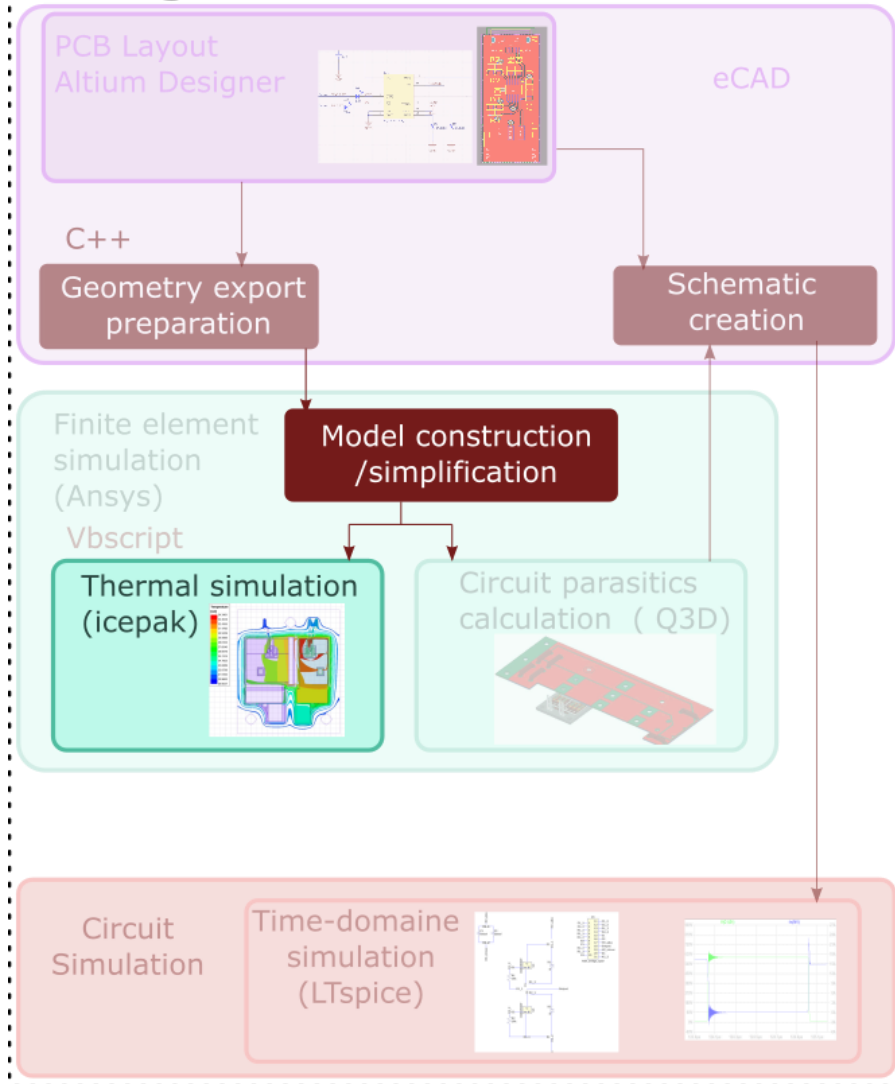


Objective of this simulation

Run the thermal transient simulation

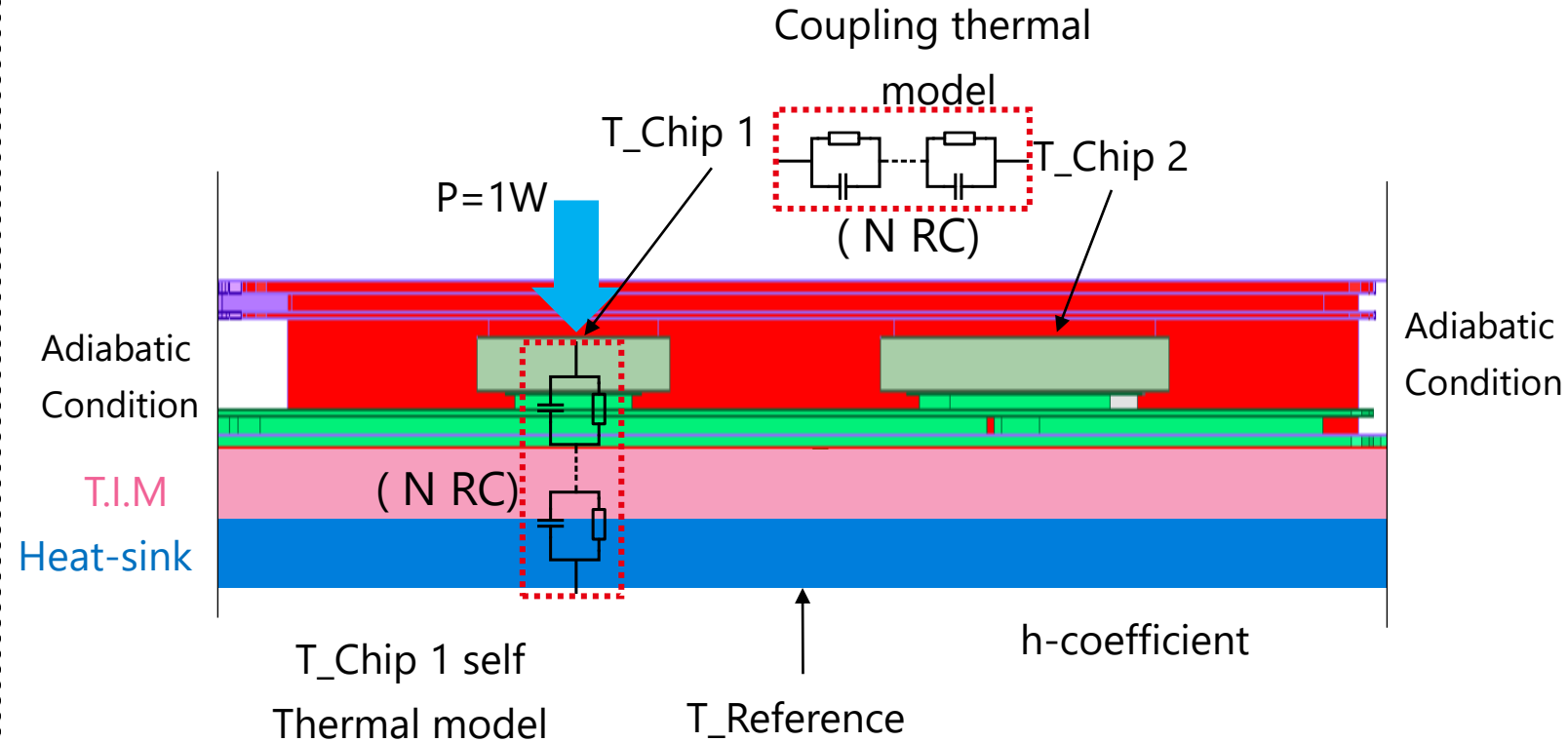


Design Toolkit

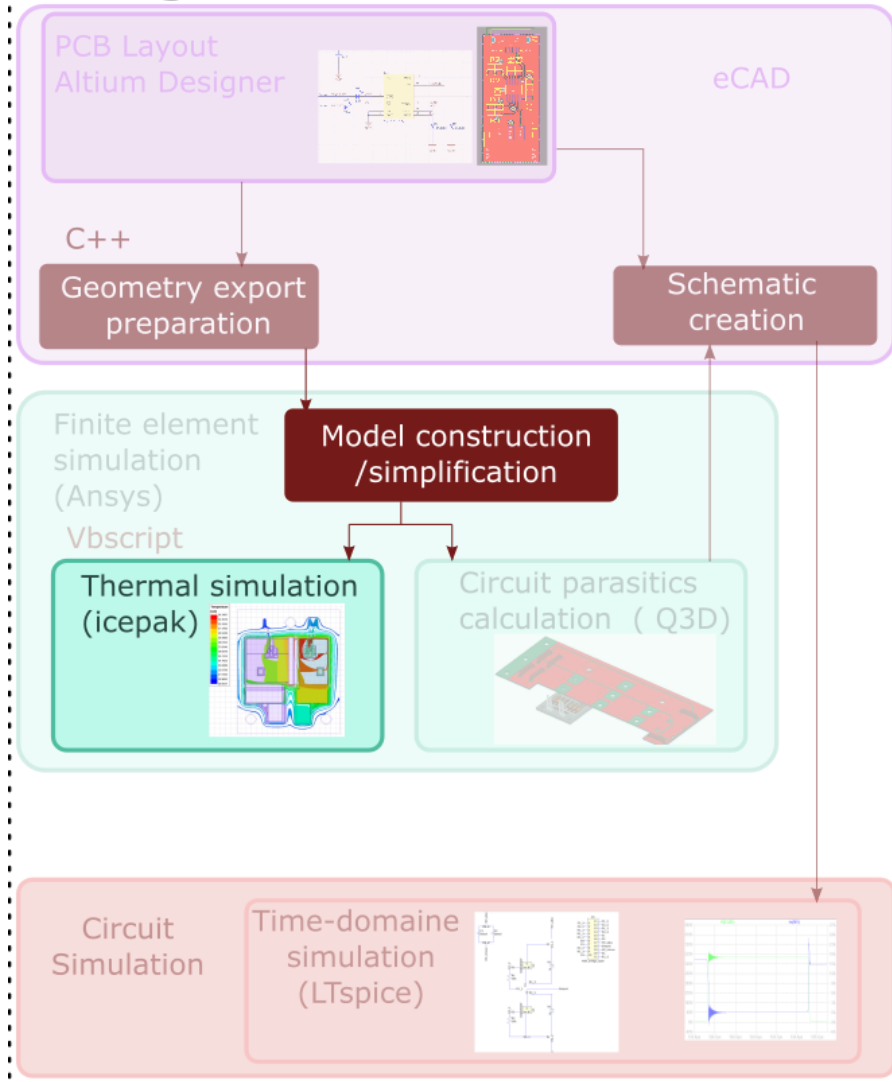


Objective of this simulation

Run the thermal transient simulation

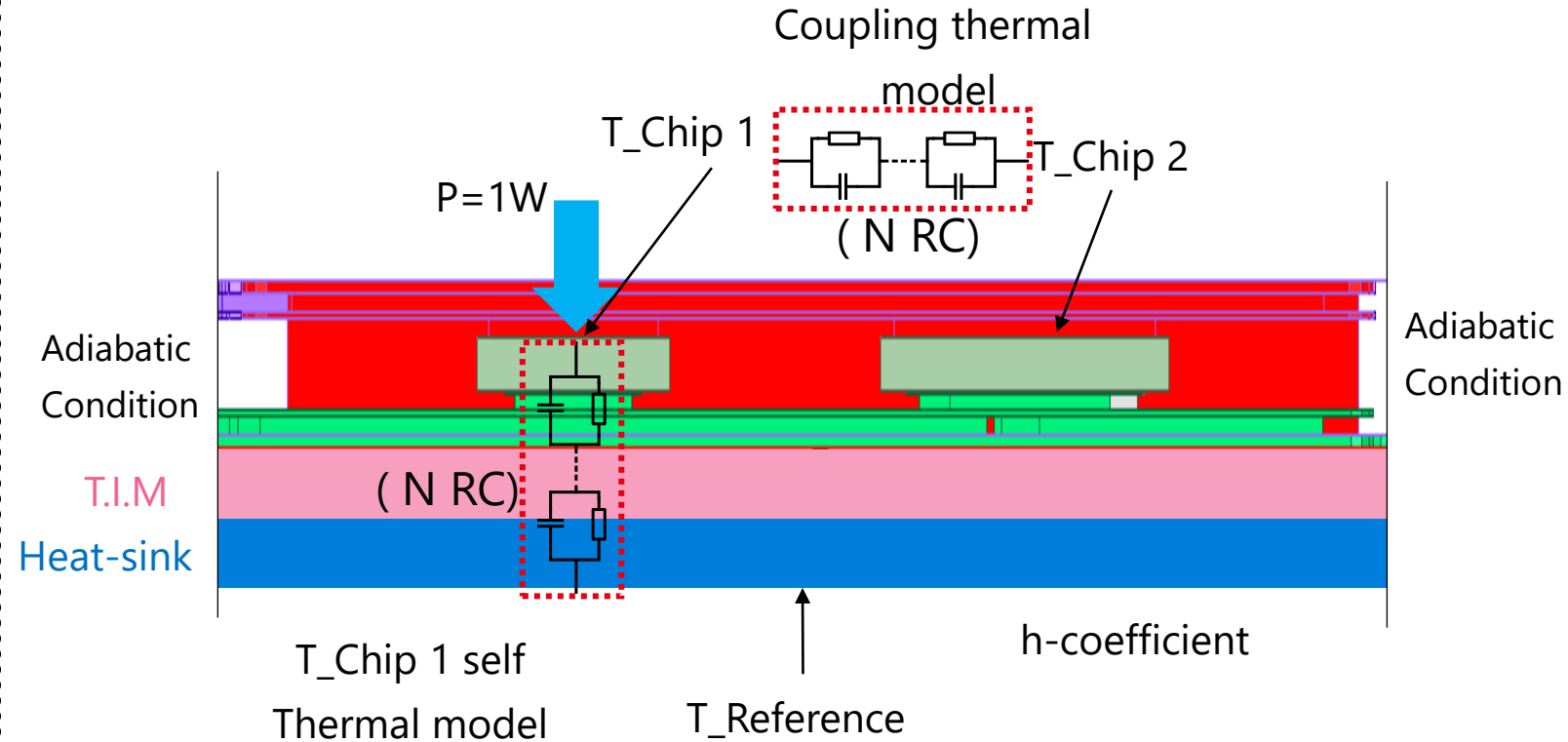


Design Toolkit



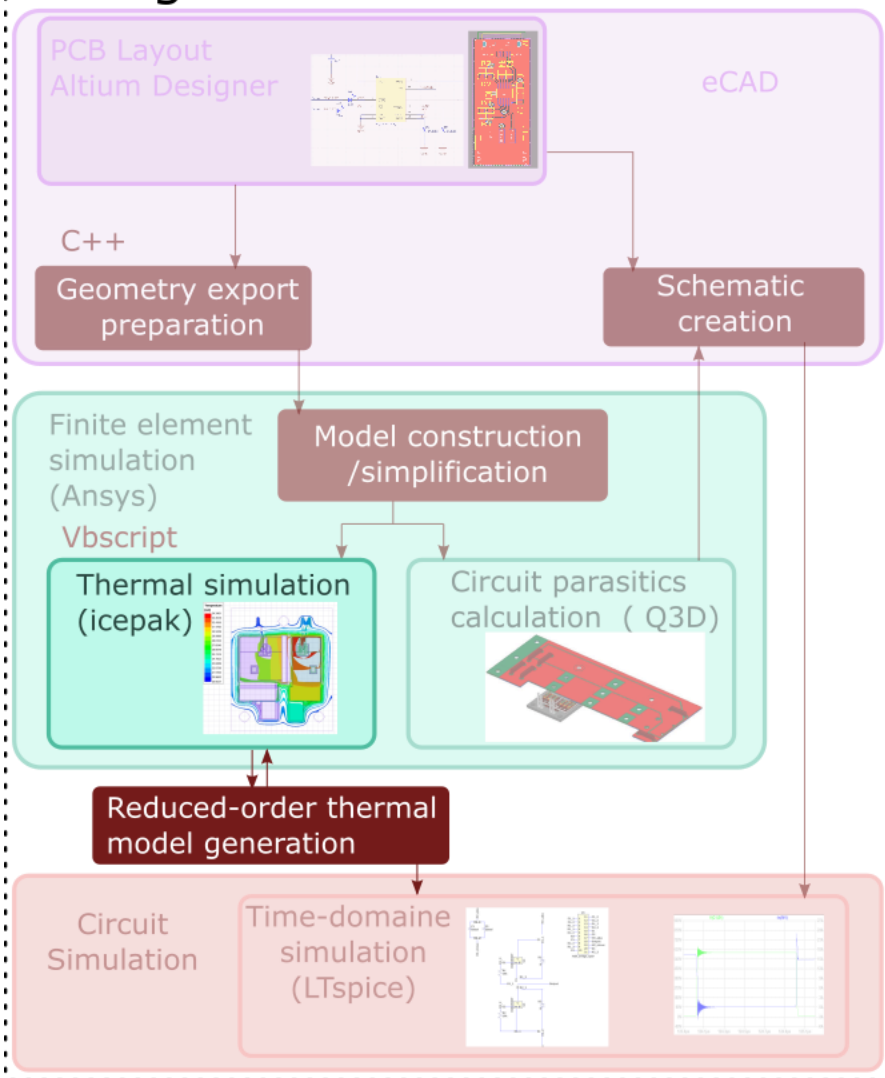
Objective of this simulation

Run the thermal transient simulation



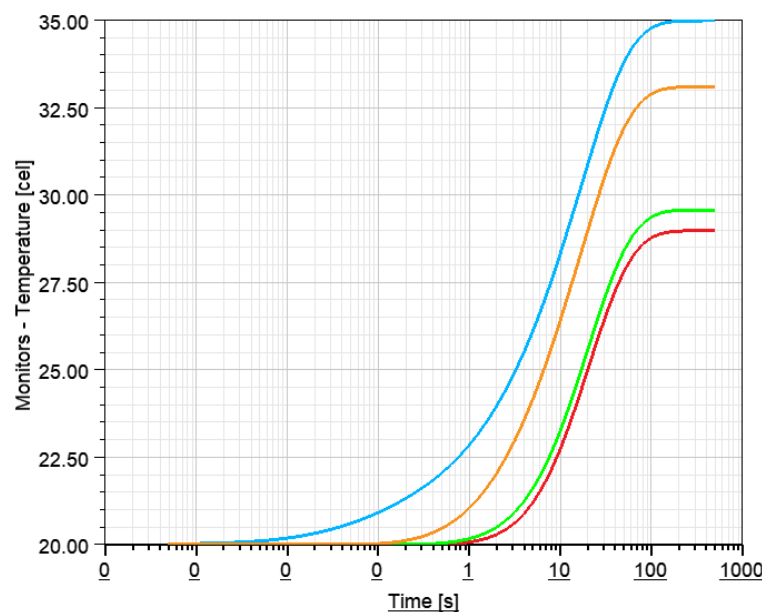
➔ N simulations to do (where 1 Chip is active and the others are off)

Design Toolkit

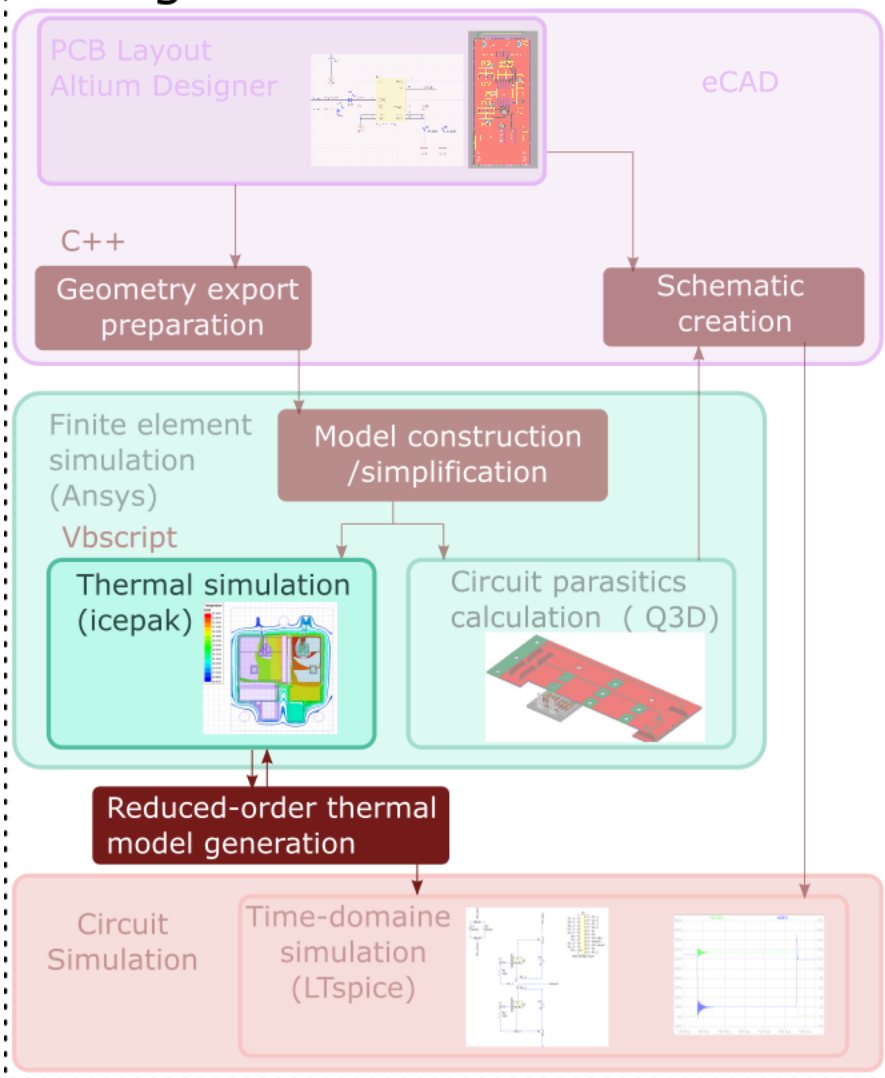


Generation of the Reduced thermal model

- From thermal transient measurement
- Self & coupling thermal model

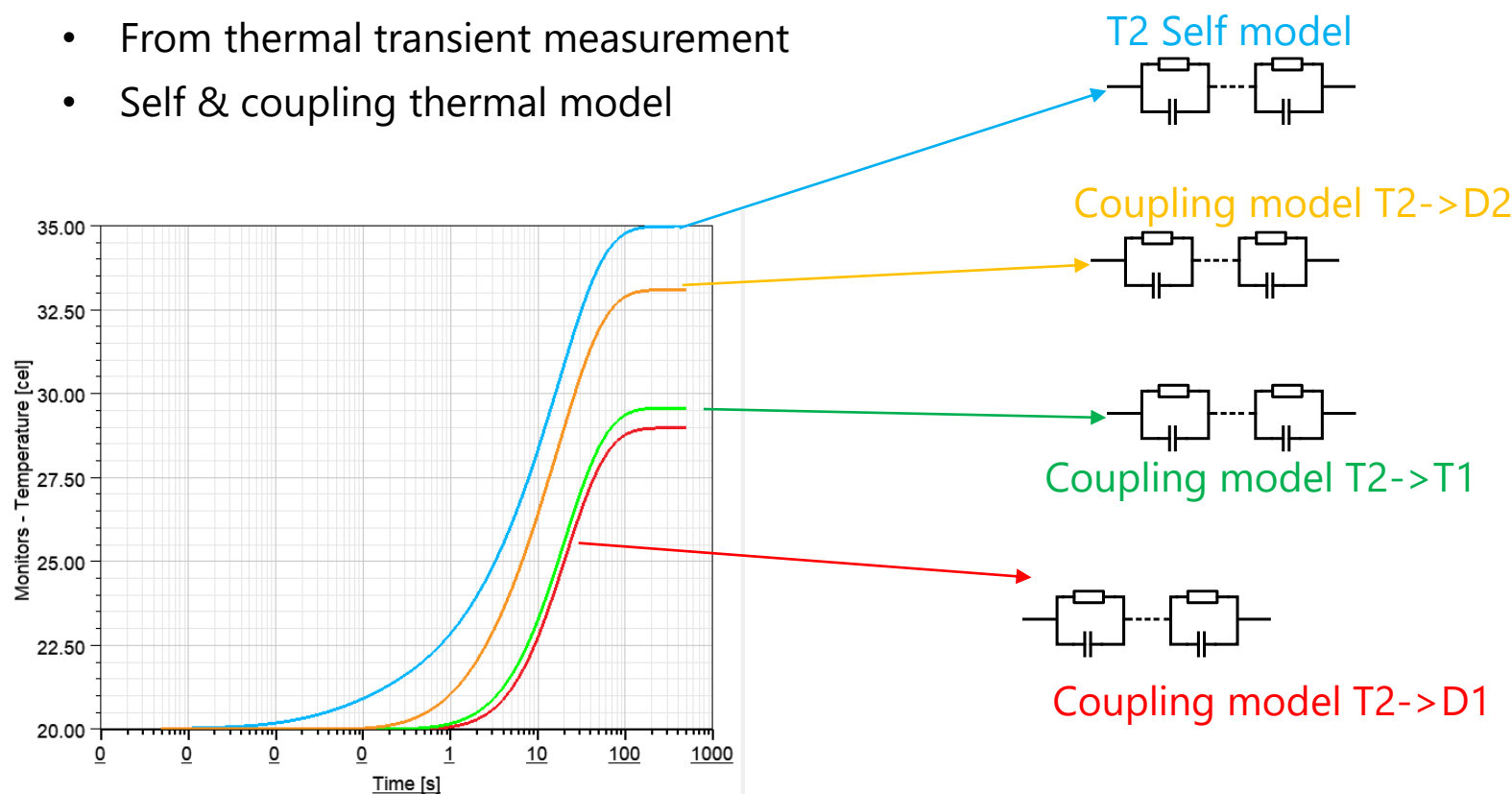


Design Toolkit

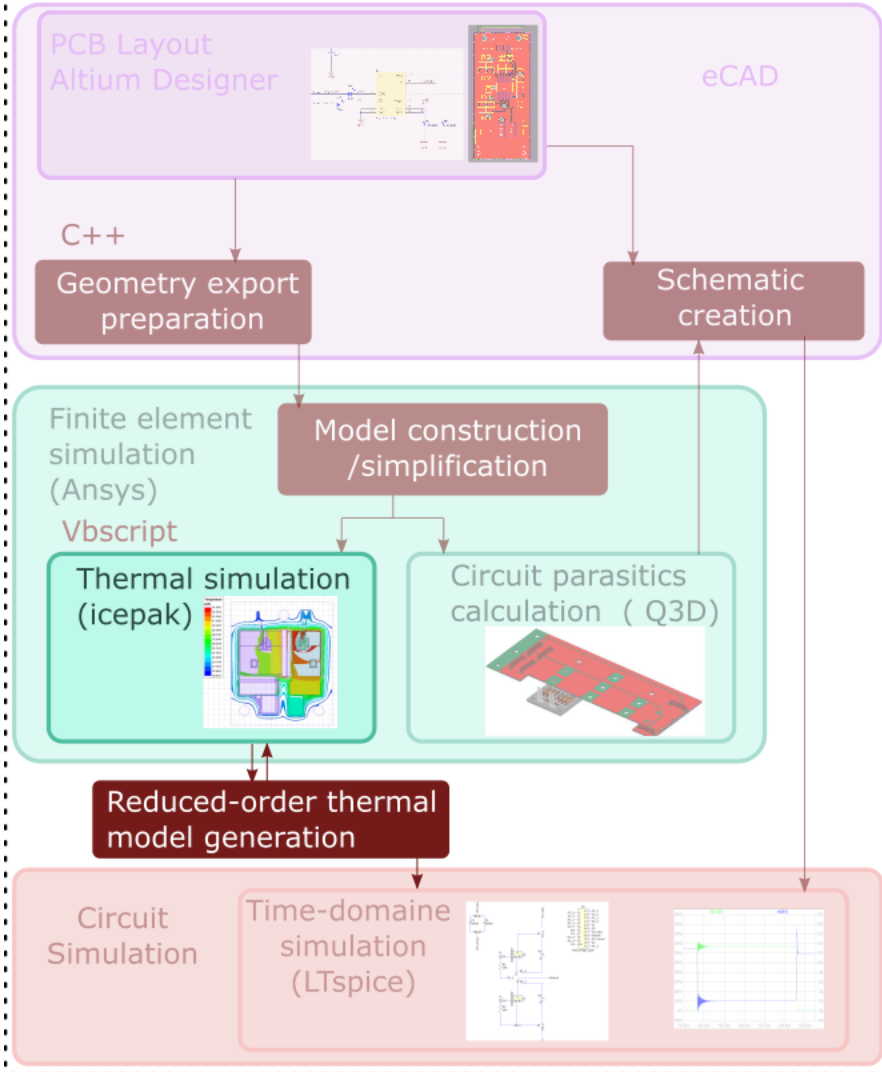


Generation of the Reduced thermal model

- From thermal transient measurement
- Self & coupling thermal model

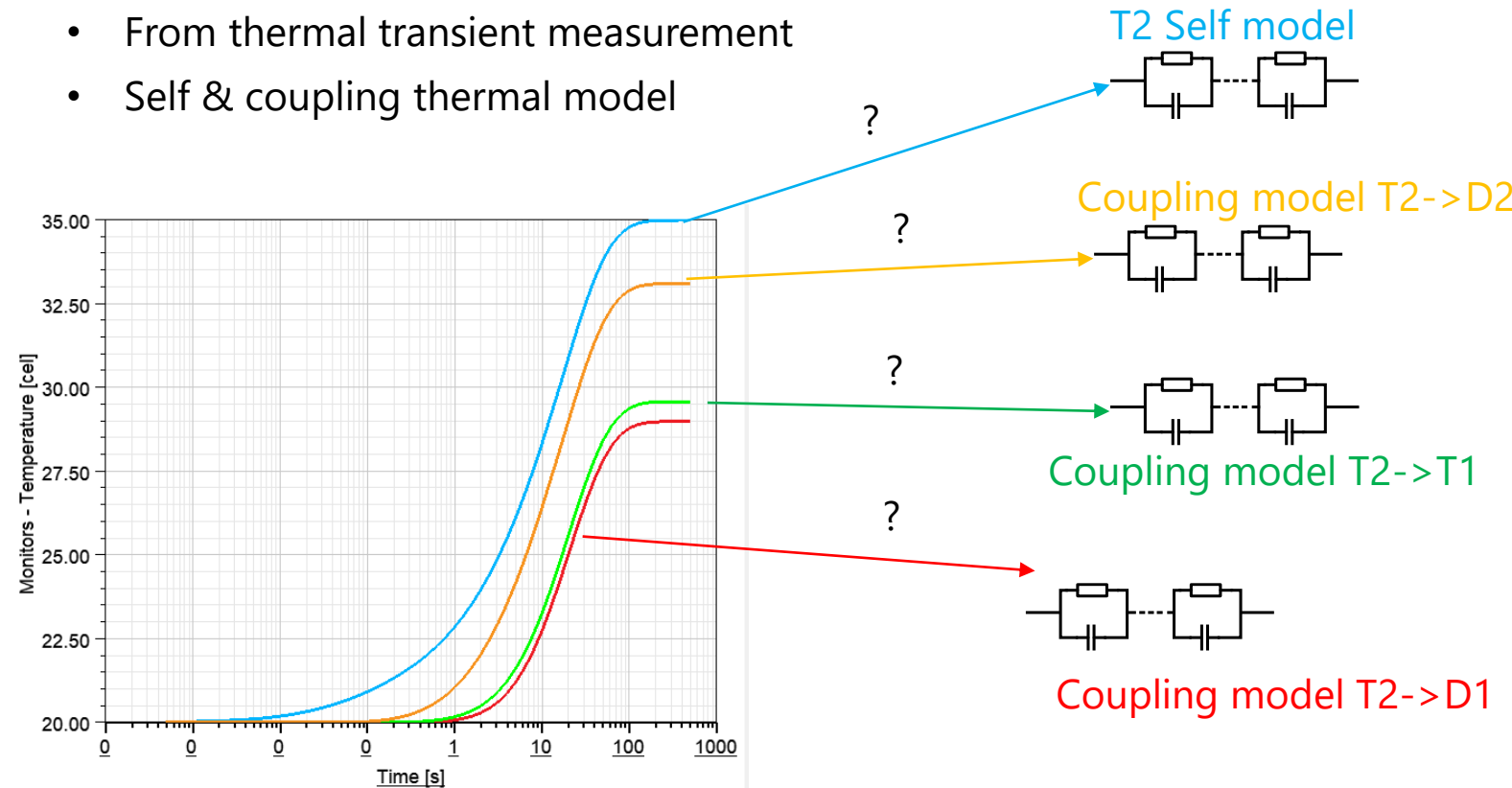


Design Toolkit



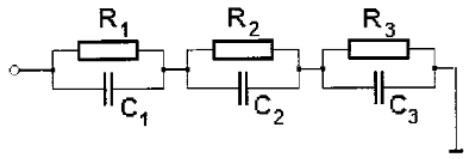
Generation of the Reduced thermal model

- From thermal transient measurement
- Self & coupling thermal model



How can we Generate such model ?

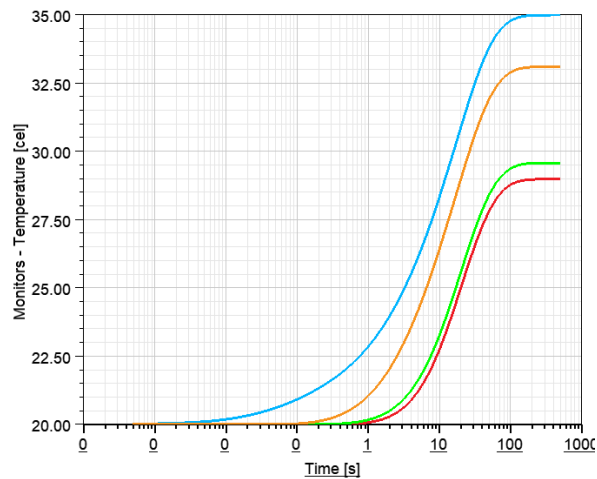
Curve Fitting methods
(Not stable enough & depends a lot from the initial conditions)



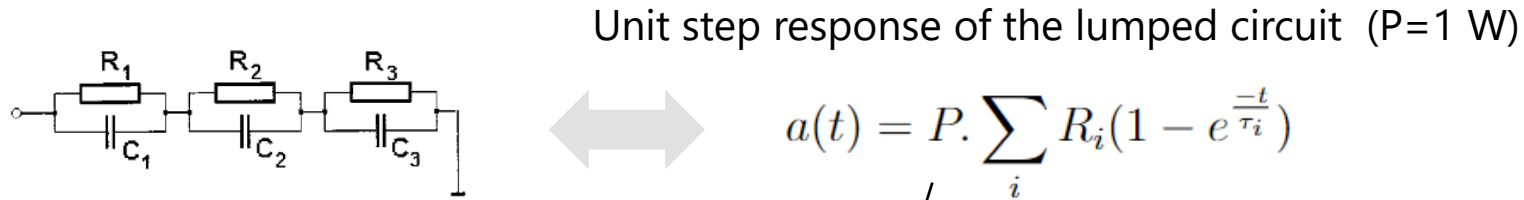
Unit step response of the lumped circuit ($P=1$ W)

$$a(t) = P \cdot \sum_i R_i (1 - e^{-\frac{t}{\tau_i}})$$

Wanted Foster model With $\tau_i = R_i \cdot C_i$



Thermal simulation output
(Icepak)

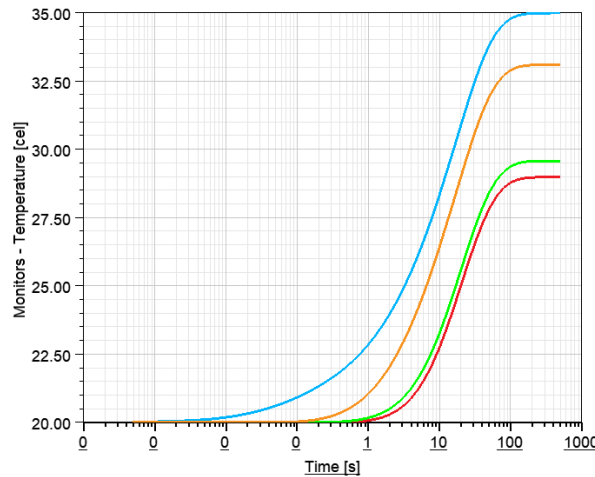
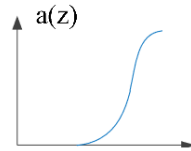


Wanted Foster model With $\tau_i = R_i \cdot C_i$

$$a(t) = P \cdot \sum_i R_i (1 - e^{-\frac{t}{\tau_i}})$$

Identification of Reduced thermal model

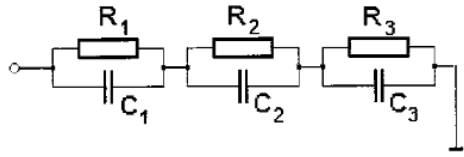
1



Thermal simulation output
(Icepak)

Used by the JEEDEC

Unit step response of the lumped circuit (P=1 W)

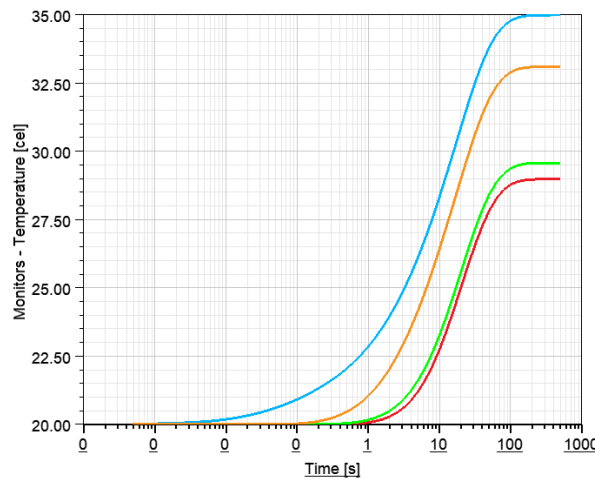
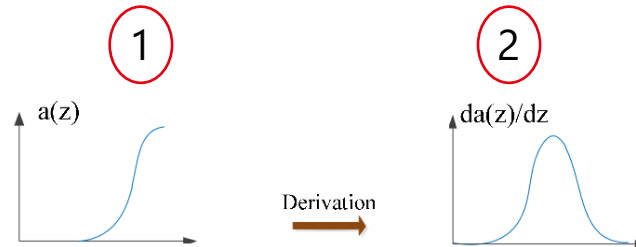


Wanted Foster model

With $\tau_i = R_i \cdot C_i$

$$a(t) = P \cdot \sum_i R_i (1 - e^{-\frac{t}{\tau_i}})$$

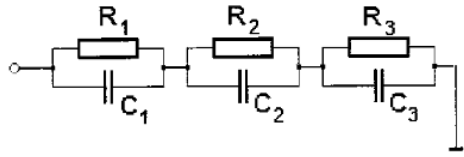
Identification of Reduced thermal model



Thermal simulation output
(Icepak)

Used by the JEEDEC

Unit step response of the lumped circuit (P=1 W)

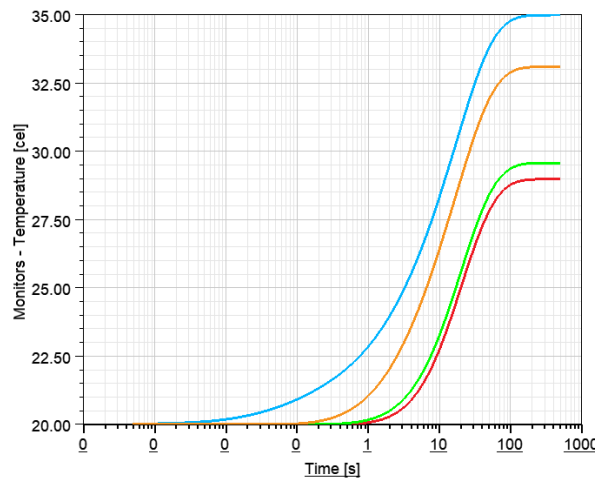


Wanted Foster model

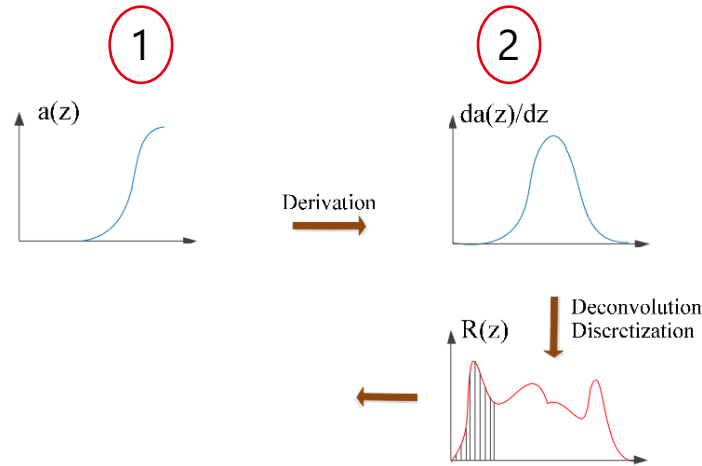
With $\tau_i = R_i \cdot C_i$

$$a(t) = P \cdot \sum_i R_i (1 - e^{-\frac{t}{\tau_i}})$$

Identification of Reduced thermal model



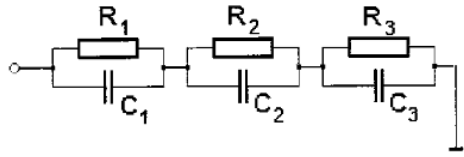
Thermal simulation output
(Icepak)



3

Used by the JEEDEC

Unit step response of the lumped circuit ($P=1$ W)

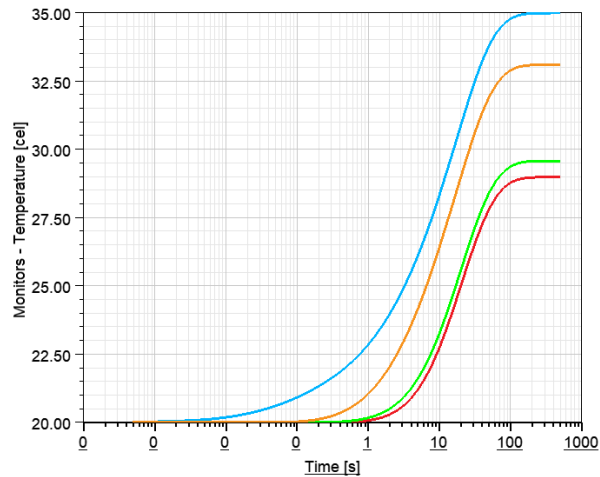


Wanted Foster model

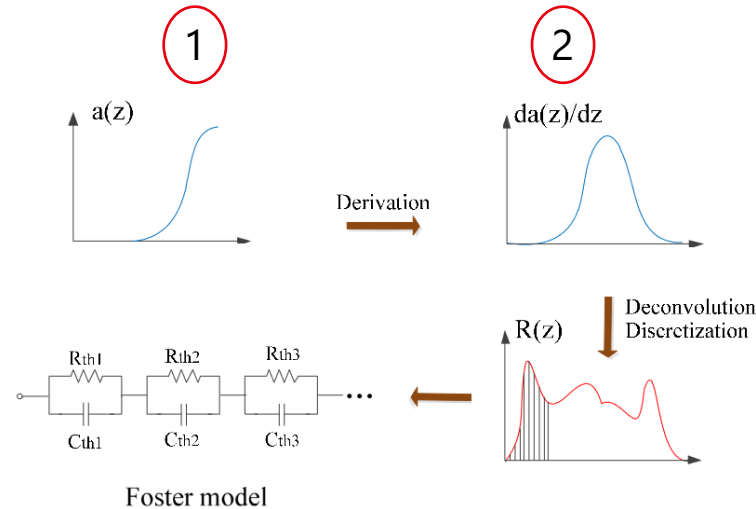
With $\tau_i = R_i \cdot C_i$

$$a(t) = P \cdot \sum_i R_i (1 - e^{-\frac{t}{\tau_i}})$$

Identification of Reduced thermal model

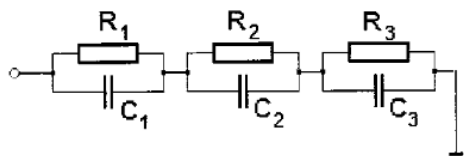


Thermal simulation output
(Icepak)



Used by the JEEDEC

Unit step response of the lumped circuit ($P=1$ W)

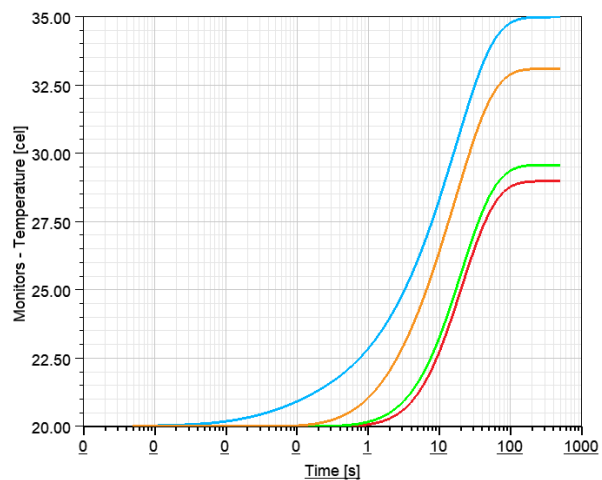


Wanted Foster model

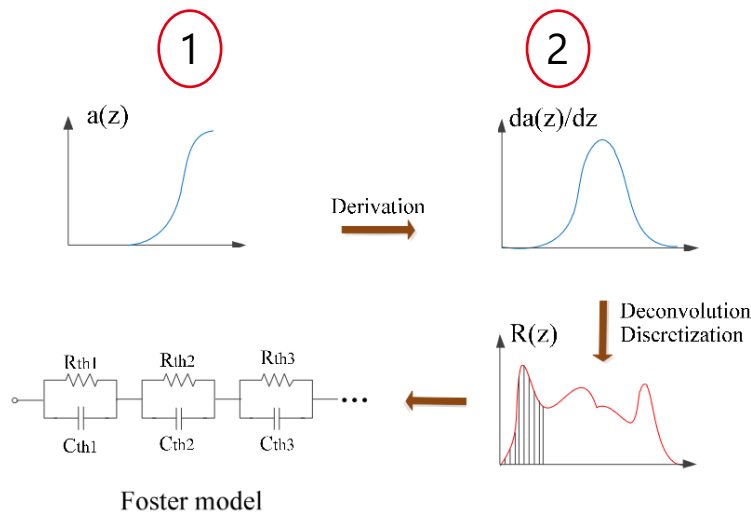
With $\tau_i = R_i \cdot C_i$

$$a(t) = P \cdot \sum_i R_i (1 - e^{-\frac{t}{\tau_i}})$$

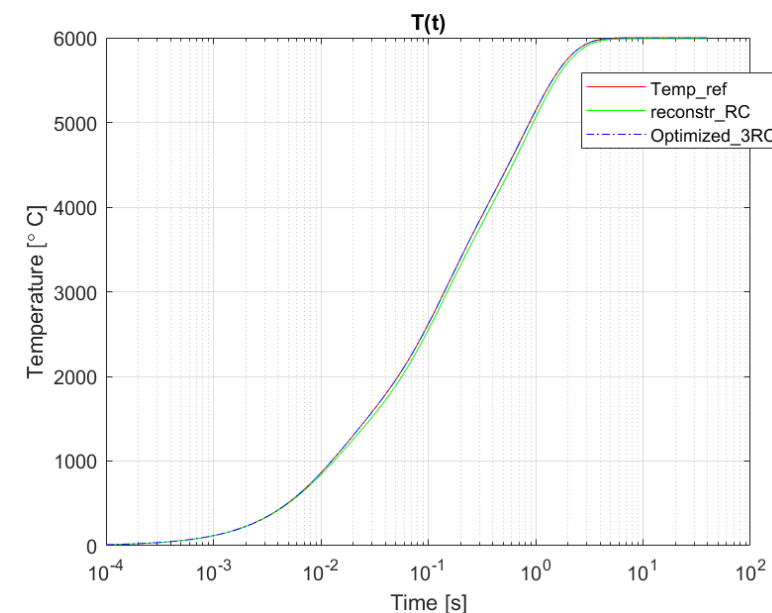
Identification of Reduced thermal model



Thermal simulation output
(Icepak)



Used by the JEEDEC



NRME = 14.4551 % → 2.2652e-06 %

Least square optimization

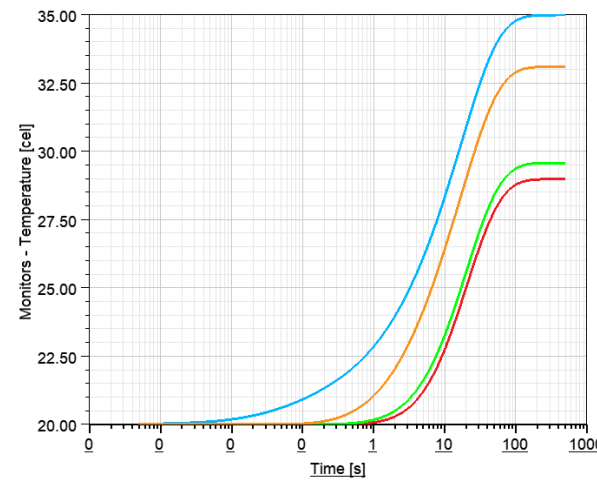
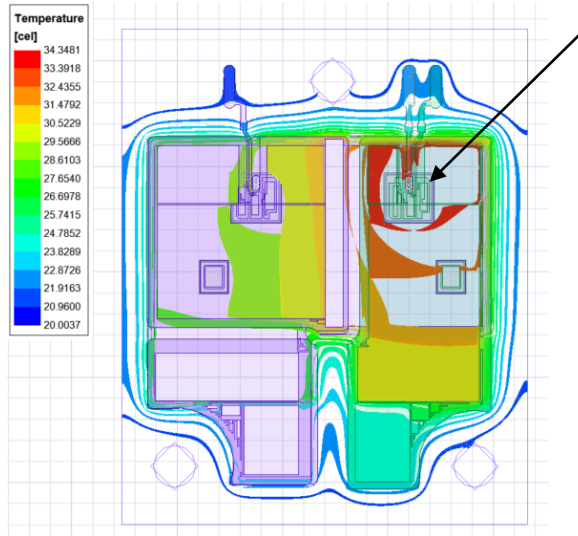
Applied on IPB1 3D model

Number of simulation = N

Where N is the number of Heat sources

T2 is active

Temperature extraction



Icepak simulation

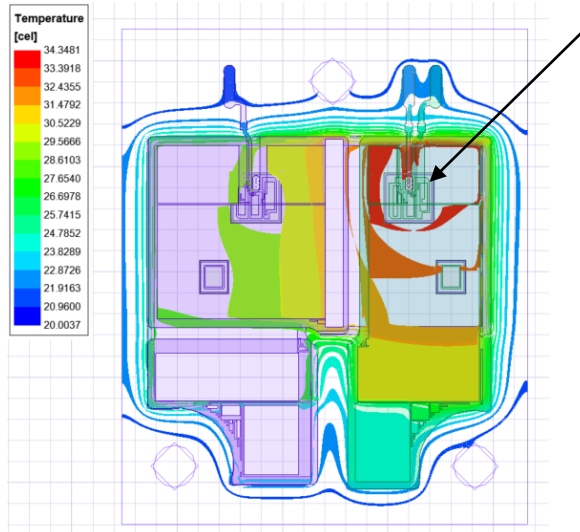
Applied on IPB1 3D model

Number of simulation = N

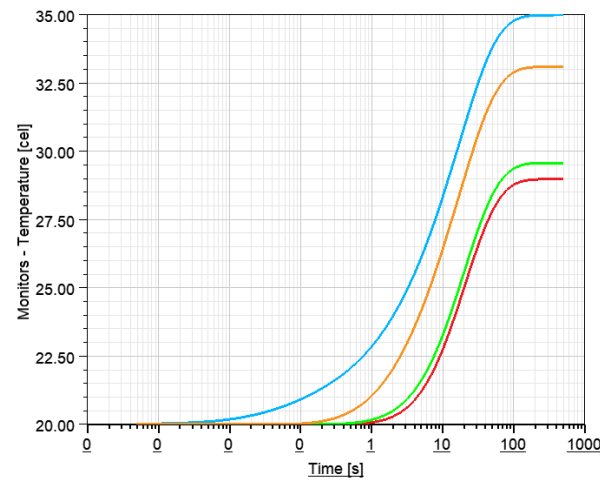
Where N is the number of Heat sources

T2 is active

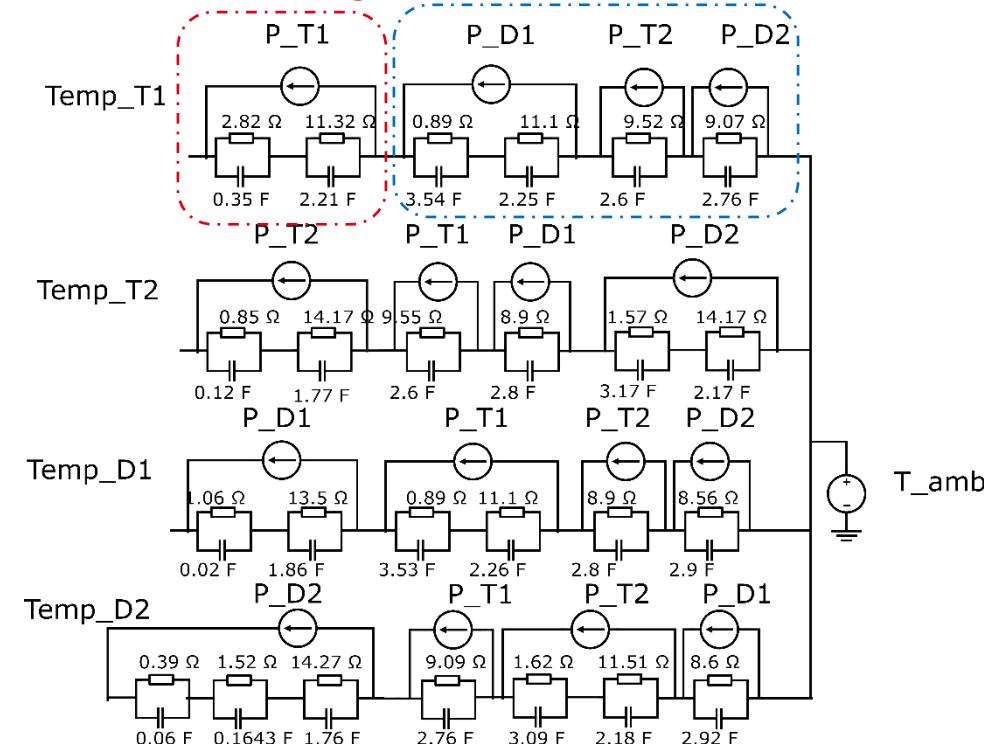
Temperature extraction



Icepak simulation



Self-heating Thermal coupling

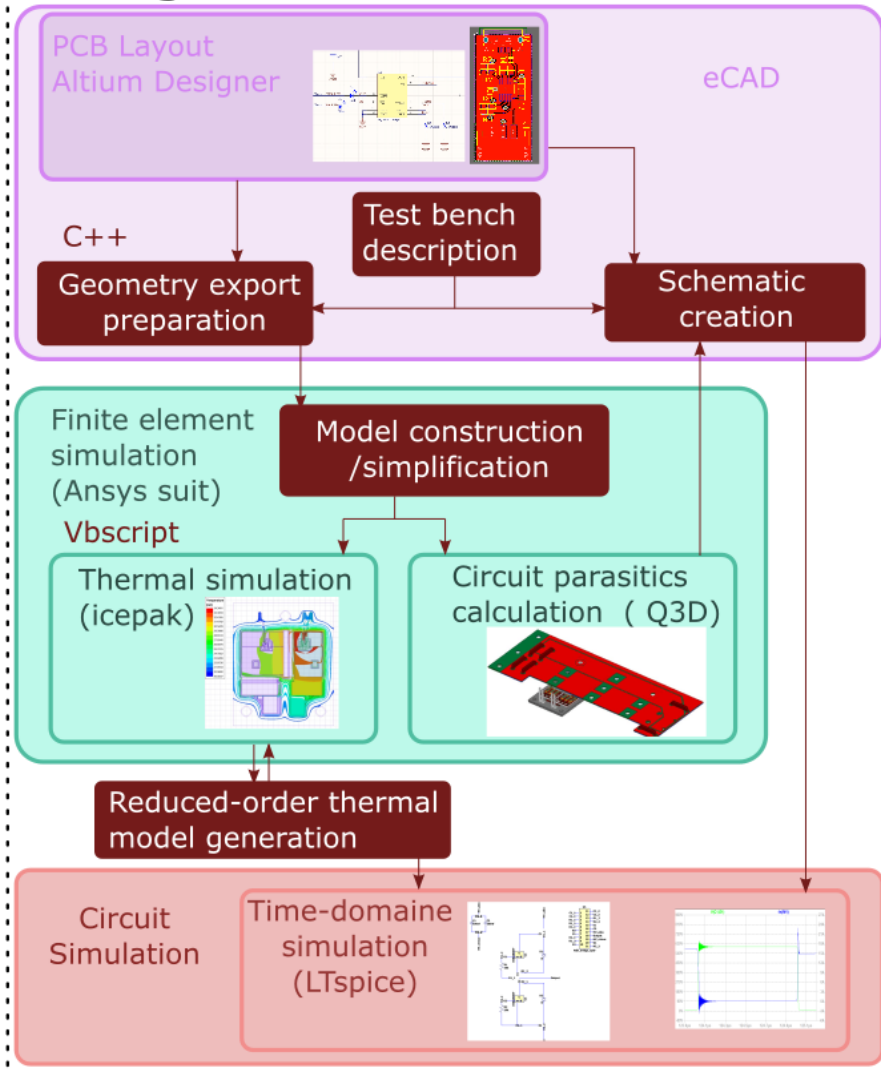


To include this thermal model to the Ltpice schematic

4

Conclusion & perspectives

Design Toolkit



Toolkit:

Electrical modelling :

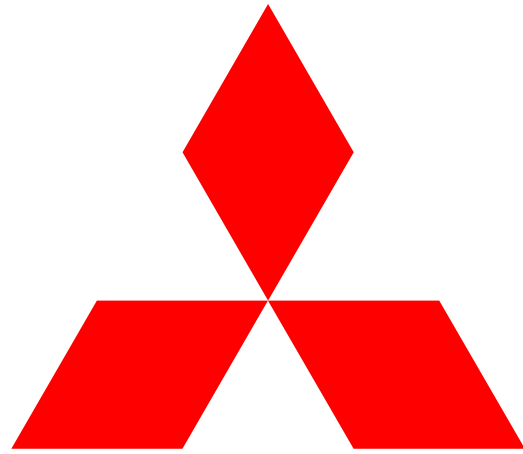
- Full workflow demonstrated on simple prototype
- Modelling of the external metal planes

Thermal modelling :

- 3D- model export/import & preparation done
- Working Zth calculation & reduced thermal model generation

Perspectives

- Validation thermal modelling approach
- Add the test bench ()
- Design a complete PCB-embedded converter (ANPC)
- Construction of the electro-thermal model
 - Validation (IPB1 & ANPC-prototype)



**MITSUBISHI
ELECTRIC**

Changes for the Better